Research into the sampling methods of digital beam position measurement (Postprint)

Authors: WU Wei-Hao, ZHAO Lei, CHEN Er-Lei, LIU Shu-Bin, AN Qi

Date: 2023-06-18T00:00:00+00:00

Abstract

A fully digital beam position monitoring system (DBPM) has been designed for SSRF (Shanghai Synchrotron Radiation Facility). As analog-to-digital converter (ADC) is a crucial part in the DBPM system, the sampling methods should be studied to achieve optimum performance. Different sampling modes were used and compared through tests. Long term variation among four sampling channels, which would introduce errors in beam position measurement, is studied, too. An interleaved distribution scheme was designed to address this issue. To evaluate the sampling methods, in-beam tests were conducted in SSRF. Test results indicate that with proper sampling methods, a turn-by-turn (TBT) position resolution better than 1 m is achieved, and the slow-acquisition (SA) position resolution is improved from 4.28 m to 0.17 m.

Full Text

Preamble

Research into the Sampling Methods of Digital Beam Position Measurement

WU Wei-Hao, ZHAO Lei,† CHEN Er-Lei, LIU Shu-Bin, and AN Qi

State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China

(Received May 5, 2014; accepted in revised form October 13, 2014; published online June 20, 2015)

A fully digital beam position monitoring system (DBPM) has been designed for the Shanghai Synchrotron Radiation Facility (SSRF). As the analog-to-digital converter (ADC) represents a crucial component in the DBPM system, sampling methods must be carefully studied to achieve optimum performance. Different sampling modes were implemented and compared through comprehensive testing. Long-term variation among the four sampling channels, which introduces errors in beam position measurement, was investigated in detail. An interleaved distribution scheme was designed to address this issue. To evaluate the sampling methods, in-beam tests were conducted at SSRF. Test results indicate that with proper sampling methods, a turn-by-turn (TBT) position resolution better than 1 μm is achieved, and the slow-acquisition (SA) position resolution is improved from 4.28 μm to 0.17 μm.

Keywords: Beam position monitor, Analog-digital conversion, Digital phase-locked loop, Interleaved distribution scheme

DOI: 10.13538/j.1001-8042/nst.26.030402

Introduction

Beam position monitors (BPMs) constitute an indispensable system in synchrotron radiation sources, measuring the transverse centroid of the beam in the storage ring, linac, linac-to-booster transfer line, full-energy booster, and booster-to-storage ring transfer line. A digital BPM (DBPM) system was designed for the Shanghai Synchrotron Radiation Facility (SSRF), a third-generation light source serving as an important platform for various scientific research domains. [Figure 1: see original paper] shows the system block diagram. The DBPM receives signals from four capacitive pickup electrodes positioned around the beam pipe, which generate fast pulses at the electron bunch repetition rate of fRF = 499.654 MHz. The input signals are first conditioned by analog radio frequency (RF) circuits in four sampling channels of the DBPM, incorporating band-pass filters and amplification circuits. Using RF amplifiers and attenuators, a dynamic range exceeding 50 dB is achieved. The 499.654 MHz RF signals are then digitized by four 14-bit ADCs operating at a sampling rate of 117.28 MHz, generating digital intermediate frequency (IF) signals at 30.5 MHz. These digital IF signals are further processed by algorithms integrated within a field-programmable gate array (FPGA) device.

As illustrated in [Figure 2: see original paper], the IF signals are converted into I and Q arrays by digital down converters (DDCs) before the amplitudes of the four input signals are calculated using the CORDIC algorithm. The beam position is then determined by employing the Δ/Σ principle:

$$X = K_x \frac{V_1 - V_2 + V_3 - V_4}{V_1 + V_2 + V_3 + V_4}$$

$$Y = K_y \frac{V_1 + V_2 - V_3 - V_4}{V_1 + V_2 + V_3 + V_4}$$

where $K_x = K_y = 10$ cm are the effective length factors in the X and Y directions, and V_{1-4} represent the amplitudes of signals in the four RF channels.

The harmonic number of the SSRF storage ring is $H = 720$, yielding a turn rate given by the machine clock frequency $f_{mc} = 499.654$ MHz$/H = 693.964$ kHz. Using a low-pass filter (LPF), slow-acquisition (SA) data are obtained from turn-by-turn (TBT) data. While TBT data are used to analyze the beam position spectrum and study position noise in the tens to hundreds of kHz range, SA data are applied to beam monitoring with a feedback loop to stabilize the beam orbit.

Since ADC performance directly affects the measurement resolution of the overall BPM system, careful consideration must be given to the sampling method. This study explores synchronization and off-tune sampling modes in the electronics design, evaluated through comprehensive testing. A digital phase-locked loop (DPLL) algorithm was deployed on an FPGA device, enabling the system to implement and switch between different sampling methods used by the ADCs. To address long-term stability issues of the ADCs and RF circuits, a switch array was designed to implement interleaved distribution of input signals among the four sampling channels. Results from on-site tests using different sampling methods are compared and analyzed.

II. Sampling Methods in the ADCs

The electron bunches produce RF signals in the BPM pickups at a frequency of $f_{RF} = 499.654$ MHz, which are fed into the DBPM inputs. These signals are modulated by a macro pulse due to the turn frequency given by $f_{mc} = 693.964\text{ kHz} = f_{RF}/H$. If the ADC sampling clock is not synchronized to the machine clock (f_{mc}), variations occur in the number of RF signals per TBT cycle, causing undue fluctuations in amplitude measurements that ultimately deteriorate position resolution. Therefore, synchronization sampling becomes mandatory for TBT data, meaning the sampling frequency (f_s) should be an integer multiple of f_{mc}:

$$f_s = \frac{M}{N} f_{mc}$$

In this case, the TBT data rate is exactly equivalent to f_{mc}. For the SSRF DBPM system, $f_s = 117.28$ MHz and $f_{mc} = 693.964$ kHz, yielding $f_{in}/f_s = 720 f_{mc}/(169 f_{mc}) = 720/169$.

Regarding SA data, the requirement for sampling frequency differs substantially. As previously mentioned, TBT data at 694 kHz are filtered by a digital LPF to obtain SA data at a much lower rate of 10 Hz. Consequently, if the sampling clock is not synchronized to the machine clock, amplitude fluctuations can be filtered out. However, due to macro pulse modulation, sidebands with a frequency interval of f_{mc} exist in the digital IF signal spectrum. In the ADCs, circuit nonlinearity causes harmonics of the digital IF signal to appear, accompanied by a similar distribution of sidebands. Some sidebands around the harmonics overlap at the digital IF signal frequency ($44 f_{mc}$), causing measurement errors at very low frequencies. This phenomenon was observed in SA measurement results from some BPM instrumentation systems, such as Libera Electron. To address this issue, f_s in Eq. (3) should be shifted by a small frequency difference Δf to relocate the harmonic sidebands outside the passband (5 Hz) of the LPF for SA data. A straightforward approach would be to set f_s completely independent from f_{mc}, but the problem is that Δf cannot be precisely controlled as f_{mc} drifts over time. This paper employs an off-tune sampling mode in which Δf is set to a specific value that can be easily modified via commands. To accommodate these sampling modes and enable switching between them, a DPLL was specially designed based on an FPGA device.

III. Synchronization and Off-Tune Sampling Based on DPLL

Conventional clock synchronization methods employ commercially available PLL chips consisting of a phase detector, charge pump, and loop filter implemented in integrated circuits. While this approach simplifies sampling clock generation circuit design, it renders switching between different sampling modes impossible. To achieve greater flexibility, we adopted a digital solution based on a modified DPLL in an FPGA device (XC4VFX100-11ff1152 from the Xilinx Virtex-4 family). The output codes from the DPLL control an external digital-to-analog converter (DAC) whose output is fed to a voltage-controlled crystal oscillator (VCXO), as shown in [Figure 3: see original paper]. With different division factors (M and N in [Figure 3: see original paper]), the frequency relationship between the output clock (f_s) and the input reference clock (f_{mc}) can be determined.

As a core component of the DPLL, the digital phase detector is categorized into linear types such as the Hogge phase detector and nonlinear types such as the Alexander phase detector (i.e., Bang-Bang phase detector). The Alexander phase detector was chosen for the DBPM system due to its superior performance and simplicity. It outputs 3-bit data indicating which of the two input signals leads the other. Its structure and principle are shown in [Figure 4: see original paper], where A, T, and B are three samples taken by three consecutive clock edges. If CLK2 leads CLK1, the first sample (A) is unequal to the last two (T and B).

This digital phase detector was implemented in the FPGA, and simulations were conducted using ISim (ISE 14.4). The results agree well with theoretical analysis ([Figure 5: see original paper]). Connecting this phase detector with the loop filter and other components in [Figure 3: see original paper] implements a complete DPLL. With this scheme, a relationship exists between the frequencies of the two input clocks of the DPLL in the locked state:

$$f_{clk2} = 2f_{clk1}$$

Considering the relationship among the machine clock, ADC sampling clock, CLK1, and CLK2 in [Figure 3: see original paper], f_s can be expressed as:

$$f_s = \frac{Mf_{mc}}{2N}$$

The relationship in Eq. (3) can then be achieved with $M = 338$ and $N = 1$.

Meanwhile, to prevent harmonic sidebands from deteriorating SA data, f_s should be shifted by a certain frequency difference Δf (i.e., the off-tune sampling mode). In this design, we implemented Δf by configuring a frequency divider with factor K:

$$K = \frac{f_{mc}}{\Delta f}$$

Thus, in off-tune sampling mode, f_s can be expressed as:

$$f_s = 169f_{mc} + \Delta f = 169f_{mc} + \frac{f_{mc}}{K} = \frac{(169K+1)f_{mc}}{K}$$

Comparing Eq. (5) with Eq. (7), off-tune sampling can be implemented by the DPLL, with the relationships among N, M, and K described by:

$$N = \frac{K}{2}, \quad M = 169K + 1$$

The next step involves determining the Δf value. The primary influence comes from the sideband ($44f_{mc}$) of the third harmonic ($37f_{mc}$) overlapping the digital IF signal. As shown in [Figure 6: see original paper], in off-tune sampling mode, the sideband of the third harmonic and the digital IF signal are shifted by $12\Delta f$ and $-4\Delta f$, respectively, achieving a total frequency interval of $16\Delta f$. To ensure effective suppression of the sideband by the LPF (5 Hz passband) for SA data, Δf must meet the requirement:

$$16\Delta f > 5 \text{ Hz}$$

Meanwhile, considering the frequency tuning range of the VCXO (VFVX 120), the upper limit for Δf is:

$$\Delta f < 5.85 \text{ kHz}$$

Combining Eqs. (9), (10), and (6), the K value ranges from 118 to 2221:

$$\frac{5 \text{ Hz}}{16} < \frac{f_{mc}}{K} < 5.85 \text{ kHz} \rightarrow 118 < K < 2221$$

In the DPLL design, K was chosen as 256, with corresponding values of $N = 128$ and $M = 43,265$. The final sampling frequency in off-tune mode can be expressed as:

$$f_s = \frac{M f_{mc}}{2N} = \frac{43265 f_{mc}}{2 \times 128} = 169 f_{mc} + \frac{f_{mc}}{256}$$

IV. Consideration of Long-Term Stability

In the DBPM system, SA data are primarily used to monitor long-term variation of beam position. The beam position is calculated from input signal amplitudes (A_1, A_2, A_3, A_4) multiplied by the gains of the four sampling channels (G_1, G_2, G_3, G_4), as shown in:

$$X = K_x \frac{V_1 - V_2 + V_3 - V_4}{V_1 + V_2 + V_3 + V_4} = K_x \frac{G_{1A}1 - G_{2A}2 + G_{3A}3 - G_{4A}4}{G_{1A}1 + G_{2A}2 + G_{3A}3 + G_{4A}4}$$

$$Y = K_y \frac{V_1 + V_2 - V_3 - V_4}{V_1 + V_2 + V_3 + V_4} = K_y \frac{G_{1A}1 + G_{2A}2 - G_{3A}3 - G_{4A}4}{G_{1A}1 + G_{2A}2 + G_{3A}3 + G_{4A}4}$$

where $K_x = K_y = 10$ cm are the effective length factors in X and Y directions; G_{1-4} are the gains of the sampling channels; and A_{1-4} are the amplitudes of the input signals.

In an ideal scenario, the four gain factors would be equal, resulting in no measurement errors in beam position calculations. However, this is not the case in real applications. While measurement errors in SA data could be easily corrected through offline calibration if differences among the four gain factors remained constant, we found that these gain factors change quite differently over time, inevitably deteriorating SA data resolution in the long term. As shown in [Figure 7: see original paper], fluctuations in SA data are evident (with a corresponding position resolution of 0.832 μm) in laboratory tests where input signals were generated by a signal source (ROHDE & SCHWARZ SMA 100A). Therefore, new methods must be applied to address this issue.

The fundamental concept involves distributing the four input signals to the four sampling channels alternately according to a specified sequence. We designed an interleaved distribution scheme using an RF switch array with the structure shown in [FIGURE:8(a)]. With different control signals, this switch array establishes corresponding signal paths between the four input ports and the four sampling channels. The control signals are generated by the FPGA and organized in a special sequence that evenly interleaves the four input signals across the four channels, as shown in [FIGURE:8(b)]. The switching frequency is designed as 5.42 kHz, which is much larger than the passband (5 Hz) of the LPF for SA data shown in [Figure 2: see original paper], allowing distortion introduced by the switching process to be easily filtered out. In this configuration, the four sampling channels have equivalent influence on processing each input signal, ensuring equality of effective gains for all input signals and greatly suppressing measurement errors caused by long-term fluctuations in the electronics.

Results from initial laboratory tests are shown in [Figure 9: see original paper]. The SA data position information over 30 minutes remains stable, with resolution around 0.032 μm, compared to 0.832 μm in [Figure 7: see original paper].

V. Test Results

To evaluate overall DBPM performance across different sampling methods, commissioning tests were conducted at SSRF ([Figure 10: see original paper]). Modulated RF signals from pickups were sent to the DBPM through four coaxial cables. After signal processing, the DBPM transmitted beam position information to a remote PC via Ethernet for further analysis.

A. Results of the TBT Data

TBT data were tested in two modes: synchronization sampling and off-tune sampling. Normalized signal amplitudes of TBT data in both sampling modes are shown in [Figure 11: see original paper]. Fluctuations are clearly visible in [FIGURE:11(b)], consistent with the discussion in Section II. Therefore, synchronization sampling was selected for TBT data, achieving a position resolution of approximately 0.61 μm.

B. Results of the SA Data

As shown in [Figure 12: see original paper], the interleaved distribution scheme significantly improves SA data performance, enhancing position resolution in a 30-minute data collection test from 4.28 μm to 0.17 μm. Similar performance can be achieved in both synchronization sampling and off-tune sampling modes, as demonstrated in [FIGURE:12(b)] and [FIGURE:12(c)], likely due to the good performance of the analog front-end in the DBPM system.

VI. Conclusion

Various sampling methods were studied to optimize DBPM performance for SSRF, including synchronization sampling, off-tune sampling, and an interleaved distribution scheme addressing long-term stability. Commissioning test results at SSRF indicate that with optimized sampling methods, TBT position resolution better than 1 μm is achieved. SA resolution can be effectively enhanced to 0.17 μm using the interleaved distribution scheme. Both TBT and SA data position resolutions exceed technical requirements.

Acknowledgment

The authors thank all SSRF collaborators who made this work possible.

References

[1] Chen S Y, Xu H J, Zhao Z T, et al. Shanghai synchrotron radiation facility. Proceeding of the Particle Accelerator Conference, 1999, 1: 209-211. DOI: 10.1109/PAC.1999.795666

[2] Yi X, Leng Y B, Lai L W, et al. RF front-end for digital beam position monitor signal processor. Nucl Sci Tech, 2011, 22:

[3] Lai L W, Leng Yong B, Yi X, et al. DBPM signal processing with field programmable gate arrays. Nucl Sci Tech, 2011, 22:

[4] Sun X D and Leng Y B. Implementation and integration of a systematic DBPM calibration with PLL frequency synthesis and FPGA. Nucl Sci Tech, 2014, 25: 020401. DOI: 10.13538/j.1001-8042/nst.25.020401

[5] Zhou H, Liu S B, Zhao L, et al. Design of the fully digital beam position monitor for beam position measurement in SSRF. 9th International Conference on Electronic Measurement & Instruments, 2009, 1: 1045-1051. DOI: 10.1109/ICEMI.2009.5273995

[6] Han Y, Zhao L, Liu S B, et al. A beam position measurement system of fully digital signal processing at SSRF. Nucl Sci Tech, 2012, 23: 75-82.

[7] Leng Y B, Zhou W M, Chen Y Z, et al. Beam instrumentation system development and commissioning in SSRF. Proceedings of European Particle Accelerator Conference, Genoa, Italy, 2008.

[8] Vismara G. The comparison of signal processing systems for beam position monitors. Proceedings of the 4th European Workshop on Diagnostics and Instrumentation for Particle Accelerators DIPAC 99, Chester, England, IT05, 1999.

[9] Yan Y B. Research of SSRF BPM data acquisition system and preliminary application. Ph.D. Thesis, Shanghai Institute of Applied Physics, Chinese Academy of Sciences, 2009, 60-63. (in Chinese)

[10] Hogge C R Jr. A self correcting clock recovery circuit. J Lightwave Technol, 1985, 3: 1312-1314. DOI: 10.1109/JLT.1985.1074356

[11] Alexander J D H. Clock recovery from random binary data. Electron Lett, 1975, 11: 541-542. DOI: 10.1049/el:19750415

[12] XILINX, http://www.xilinx.com/support/documentation/application_{notes}/xapp854.pdf XAPP854 reference (DPLL) design, Digital phase-locked (v1.0).

[13] Libera Electron User Manual 2.04. Instrumentation Technologies, 2009.

Note: Figure translations are in progress. See original paper for figures.