Design and measurement of signal processing system for cavity beam position monitor postprint

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Abstract

In this paper, to achieve output signal processing for cavity beam position monitors (CBPM), we develop a signal processing system based on a digital intermediate frequency receiver architecture, which consists of a radio frequency (RF) front end and a high-speed data acquisition board. The beam position resolution of the CBPM signal processing system is superior to 1 m. Two signal processing algorithms, fast Fourier transform (FFT) and digital down converter (DDC), are evaluated offline using the MATLAB platform, achieving position resolutions of 0.31 m and 0.10 m, respectively, for CW input signals at –16 dBm. The DDC algorithm, due to its good compatibility, is downloaded into the FPGA to enable online measurement, achieving a position resolution of 0.49 m due to truncation error. The entire system operates reliably and its performance meets the design target.

Full Text

Preamble

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Design and Measurement of Signal Processing System for Cavity Beam Position Monitor

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Abstract
In this paper, we develop a digital intermediate frequency receiver architecture for the signal processing of cavity beam position monitors (CBPM). The

system consists of a radio frequency (RF) front end and a high-speed data acquisition board, achieving a beam position resolution superior to 1 m. Two signal processing algorithms—fast Fourier transform (FFT) and digital down converter (DDC)—are evaluated offline using the MATLAB platform. Both methods achieve position resolutions of 0.31 m and 0.10 m, respectively, for continuous-wave input signals at –16 dBm. Due to its excellent compatibility, the DDC algorithm is downloaded into an FPGA for online measurement, achieving a position resolution of 0.49 m due to truncation error. The entire system operates reliably and meets the design targets.

Key words: Cavity beam position monitor, RF front end, Digital down converter, Fast Fourier transform, FPGA

Introduction

Cavity beam position monitors (CBPMs) are critical components for free-electron laser (FEL) and linear collider (LC) facilities, where submicron or even nanometer-level position resolution is required when the beam passes through long undulator sections or interaction points in LCs [**?**, **?**]. CBPMs offer greater potential than electrostatic stripline BPMs for achieving nanometer-scale resolution. A prototype CBPM with high quality factor has been installed on the Shanghai deep ultraviolet FEL (SDUV-FEL), a high-gain harmonic generation facility. Beam tests using a wide-bandwidth oscilloscope have demonstrated the utility of CBPM outputs and operational principles for designing signal processing systems [**?**], though these cannot achieve optimal resolution for FEL or LC applications due to limitations in analog-to-digital converters (ADCs). In the future, dedicated digitizers will process RF signals directly using ADC techniques, but currently RF signals must be downconverted using analog electronics before digitization.

Both heterodyne and homodyne methods are employed in radio techniques for signal frequency conversion, though each can degrade system performance. Heterodyne receivers require an additional filter before the mixer to reject image frequencies, and their two-stage down-conversion architecture increases component count, hindering system integration. Homodyne receivers directly convert RF signals to baseband, but imbalances or mismatches between in-phase/quadrature-phase (I/Q) channels introduce errors, and local oscillator (LO) leakage into the mixer RF port creates direct current interference. However, advances in data converter and radio technology have simplified complex receiver designs, with high-precision digitizers capable of several hundred megahertz now commercially available.

This paper applies digital receiver architecture [**?**] to the RF front end of the signal processing system. RF signals are directly downconverted to a low intermediate frequency (IF), moving I/Q demodulation from the analog to the digital domain. All data conversion processes are implemented on a commercial ICS1554-002 data acquisition board (GE Corp.) [**?**], which features a high-

precision 16-bit ADC with sampling rates up to 160 MSPS and a Virtex-5 FPGA device. Digital signal processing algorithms enable pulse-by-pulse beam position measurement within a single shot containing many micropulses.

2 System Setup

The CBPM signal processing system comprises a dedicated RF front end and a commercial digitizer. The quality factor (Q) is a key parameter in CBPM design, being inversely proportional to output signal intensity and bandwidth while directly proportional to the decay time of the output signal [**?**]. Consequently, high-Q and low-Q designs require different RF front-end approaches. We developed two CBPM prototypes with high and low Q factors, with a dedicated RF front end capable of accommodating both designs through interchangeable IF low-pass filters (LPFs) [**?**].

The RF front end, based on RF receiver architecture, is essential for converting RF signals to IF. For CBPMs with high/low Q factors, IF and LPF selection are particularly critical. Table 1 summarizes the detailed system design parameters.

For high-Q prototypes, the signal bandwidth is narrow but the cavity output signal intensity is low, necessitating high-performance RF front ends to improve signal strength. Additionally, digital signal processing (DSP) algorithms can process sufficient samples to enhance the noise level within a certain bandwidth. For low-Q prototypes, the CBPM output intensity is high and the bandwidth is very wide, resulting in lower RF front-end performance requirements compared to high-Q CBPMs. However, the time constant of low-Q CBPM outputs is small (directly proportional to Q), providing insufficient samples for FFT techniques. Consequently, only the DDC algorithm is suitable for low-Q systems.

2.1 RF Front End

The RF signal from the CBPM is converted to IF and digitized by the commercial board at up to 160 MHz sampling rate (Fig. 1) [**?**]. RF signals from the CBPM first pass through a band-pass filter (BPF) with a center frequency of 4.7 GHz (5.712 GHz for the alternative prototype), 100 MHz bandwidth, and 60 dB stop-band attenuation to suppress harmonics. The filtered signals then enter a low-noise amplifier (LNA) with 45 dB gain to achieve a broader dynamic range. A mixer with 3.7–7 GHz input bandwidth performs RF-to-IF conversion using high LO power. In the LO channel, an amplifier with a high 1-dB compression point output power is added before the power divider to meet the mixer LO input requirements. In the IF section, a 32 MHz bandwidth LPF (11 MHz for the alternative prototype) removes high-order mixer harmonics. An IF amplifier provides final gain adjustment to satisfy ADC input requirements, and the final LPF serves as an anti-aliasing filter to suppress amplified harmonics.

2.2 Front End Bunch Test

To achieve position resolution superior to 1 m, the RF front-end noise level must be below –70 dBm and amplitude stability better than 4%. During testing, input power ranging from –100 dBm to –40 dBm was generated using a signal generator and power divider to produce three-channel RF signals for the RF front end. The front-end output was sampled by an ICS1554A-002 board at 160 MHz sampling rate, with all data processed in MATLAB. Fig. 2 shows the test diagram, and Fig. 3 presents the gain linearity test results. As shown in Fig. 4, the three-channel linearity error is less than 2% for input power above –80 dBm, with noise level below –90 dBm and amplitude error less than 0.4% (RMS), meeting design specifications.

3 Algorithm Design

Extracting beam position from raw CBPM signals requires precise demodulation of amplitude and phase from digitized waveforms. In the time domain, output signals are nominally exponentially decaying sine waves. Two independent methods—fitting and DDC—determine amplitudes and phases in the time domain [**?**, **?**]. In the frequency domain, FFT techniques extract calibrated amplitudes and phases. To weaken harmonic influence in the time domain and improve position resolution, we adopted FFT-based signal processing. Before FFT, a FIR filter reduces harmonics induced by the RF front-end frequency mixer and lowers the noise level. Fig. 5 shows the processing algorithm diagram. Since single-pulse position measurement within a shot containing many micropulses is required, all algorithms must be implemented on the FPGA device using hardware description language (HDL). Therefore, we focused on DDC and FFT algorithms.

3.1 Fitting

The raw waveform V(t) from one CBPM output channel can be expressed by Eq. (1) [**?**]:

$$V(t) = V_0 + Ae^{-0.5t/\tau}\sin[\omega t + \phi] \quad (1)$$

where A and ϕ are the amplitude and phase, V_0 is the ADC pedestal value, and τ and ω are the decay time constant and angular frequency. When fitting for A and ϕ, τ and ω are fixed parameters determined from calibration data for each channel, with their average values used as the fixed τ and ω.

3.2 DDC

The CBPM output in the time domain is also processed using the DDC algorithm, where V(t) from a given channel is multiplied by a complex LO at the same ω, converting the raw signal to baseband. A digital low-pass filter,

designed as a symmetric finite impulse response (FIR) filter, reduces high harmonics and noise by convolving the complex signal with a specific-coefficient, specific-bandwidth FIR LPF. The demodulated signal is described by Eq. (2) [**?**, **?**]:

$$y_{DDC}(t) = [(y_{digital} - y_0)e^{i\omega_{DDC}t}] * \text{Filter} \quad (2)$$

where y_{digital} is the raw ADC signal, y_0 is the ADC pedestal value determined by averaging ADC samples before the beam passes through the cavity, and ω_{DDC} is the angular frequency equal to the IF from the RF front end. The Filter term represents the FIR coefficient vector. The acquired baseband signal peak and its corresponding phase determine beam position and offset direction.

3.3 FFT

The FFT algorithm demodulates amplitude in the frequency domain. In testing, a –16 dBm RF signal was input to the antenna while the platform moved from 0 m to 100 m in 2- m steps. At each position, 100 samples were acquired, with each sample containing 256 sampling points [**?**]. Both fitting and DDC algorithms demonstrated equivalent performance [**?**]. However, the fitting algorithm requires extensive runtime and is difficult to implement on FPGA, so DDC and FFT algorithms were adopted for demodulating the calibration scale factor and evaluating position resolution. The DDC algorithm, applicable to both high-Q and low-Q CBPM systems, was implemented on FPGA devices.

4 Bench Test

Systematic signal processing performance was evaluated using a dedicated mobile platform with submicron-level single-step resolution. A newly manufactured cavity was mounted on the platform, and RF signals from a signal generator were input to the cavity via an antenna, then fed to the electronics through the cavity output.

4.1 DDC Algorithm Test

The DDC algorithm was applied to data sampled by the commercial digitizer to obtain the calibration scale factor (Fig. 6). The platform was positioned at a specific offset from the cavity center to meet ADC SNR requirements, and 1024 samples were acquired to evaluate system position resolution (Fig. 7), achieving a resolution of 0.31 m.

4.2 FFT Algorithm Test

The same procedure used in the DDC test was applied to the FFT test. The calibration scale factor showed smaller error bars for FFT than for DDC (Fig.

8). Using identical test methods, the FFT algorithm achieved a 0.1- m resolution (Fig. 9).

4.3 FPGA Algorithm Test

To enable single-pulse position measurement, processing algorithms were implemented on the FPGA device using efficient hardware. Hardware algorithms employing parallel operation improve processing speed at the cost of hardware resources. The DDC algorithm on FPGA was implemented using the coordinate rotation digital computer (CORDIC) algorithm [**?**, **?**] rather than the conventional quadrature-mixing method, which consumes substantial RAM resources for sine/cosine lookup tables and requires multiplier pairs. The CORDIC algorithm uses only shifts and additions. The FIR filter based on Xilinx FIR IP core [**?**] removes the up-converted component, while amplitude and phase demodulation in coordinate conversion (COC) uses the vectoring mode of CORDIC. Fig. 10 shows the FPGA algorithm architecture. Using the same test method, the calibration scale factor is shown in Fig. 11, and Fig. 12 demonstrates a 0.49- m resolution—slightly worse than the DDC algorithm due to data-bit truncation error.

5 Conclusions

This study accomplished a complete CBPM signal processing system with relevant digital algorithms implemented. In bunch tests, the DDC algorithm achieved 0.31- m position resolution, while the FFT algorithm reached 0.10- m resolution at –16 dBm input power, meeting beam position diagnostic requirements for the Shanghai soft X-ray FEL facility. Preliminary FPGA algorithm implementation and bunch testing yielded slightly worse resolution than digital algorithms due to truncation errors. Future work will focus on beam testing of the complete CBPM system.

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Note: Figure translations are in progress. See original paper for figures.