Nupix-H2: Monolithic Active Pixel Detector Circuit Design

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Abstract

In nuclear and particle physics experiments, vertex and tracking detectors are primarily utilized to acquire information such as the position, energy, and time of collision particles. In recent years, Monolithic Active Pixel Sensors (MAPS) have garnered significant attention in the detector field. Based on MAPS technology, a chip designated as Nupix-H2 will be designed, featuring a domestic 130 nm CMOS process, pixel array dimensions of 128 rows × 128 columns, an individual pixel area of 22 m × 22 m, and employing a Rolling Shutter readout scheme for row-by-row scanning with column-wise sequential output of information from each pixel unit at a scanning frequency of 40 MHz. To validate the feasibility of this chip, this work presents a 1-row × 16-column test array Nupix-H2-, wherein the pixel array' s energy information is read out via a charge-sensitive amplifier, time information is measured through a counter, and the system enables automatic reset. Simulation results indicate that the pixel array achieves an ENC of less than 30 e-, an energy resolution of approximately 5%, and a time resolution of less than 25 ns.

Full Text

Design of Nupix-H2- Monolithic Active Pixel Detector Circuit

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Abstract

In nuclear and particle physics experiments, vertex and tracking detectors are primarily used to acquire position, energy, and timing information of collision particles. In recent years, Monolithic Active Pixel Sensors (MAPS) have attracted widespread attention in the detector field. Based on MAPS technology, a chip named Nupix-H2 will be designed using a domestic 130 nm CMOS process, featuring a pixel array of 128 rows × 128 columns with individual pixel dimensions of 22 m × 22 m. The chip employs a Rolling Shutter readout scheme with row-by-row scanning, sequentially outputting information from each pixel unit column by column at a scanning frequency of 40 MHz. To verify the feasibility of this chip, a test array named Nupix-H2- with dimensions of 1 row × 16 columns has been designed. The energy information of this pixel array is read out through a charge-sensitive amplifier, while timing information is measured by a counter, and the system can achieve automatic reset. Simulation results demonstrate that the pixel array achieves an Equivalent Noise Charge (ENC) of less than 30 e^-, an energy resolution of approximately 5%, and a time resolution better than 25 ns.

Keywords: Pixel detector; CMOS pixel circuit; MAPS; Particle physics

1 Introduction

As China' s leading platform for heavy ion scientific research, the Heavy Ion Research Facility in Lanzhou (HIRFL) and the High Intensity Heavy-ion Accelerator Facility (HIAF) have driven the development of novel detector technologies for heavy ion physics and applications [?, ?]. In recent years, the Institute of Modern Physics has begun constructing a new generation of large-scale physics experimental facilities, represented by the Electron-Ion Collider in China (EicC), based on the HIAF complex [?]. With the rapid development of these scientific facilities, the physics experiments conducted on them impose higher performance requirements on vertex and tracking detectors. Monolithic Active Pixel Sensor (MAPS) technology, which integrates the sensor and front-end readout electronics on the same silicon die, offers advantages including high sensitivity, high spatial resolution, low noise, and low power consumption [?, ?, ?], and has consequently been adopted in multiple high-energy physics particle detectors [?, ?].

However, most current MAPS only record the position information of particle hits. To meet physicists' demands for comprehensive particle performance studies, it is necessary to further improve the detector's timing and energy resolution. This design completes the verification chip Nupix-H2- based on a domestic 130 nm CMOS process, enabling simultaneous high-precision measurement of position, energy, and timing information of incident radiation particles.

2 Nupix-H2- Structure and Working Principle

The basic structure of Nupix-H2- is shown in [Figure 1: see original paper]. The Nupix-H2- chip consists of 1 row × 16 columns, with each pixel measuring 22 m × 22 m. Each pixel features both energy and timing readout channels, capable of measuring input charges in the range of 0.1–10 ke^{-}. The energy channel comprises a charge-sensitive amplifier, source follower circuit, and analog readout buffer circuit. The timing channel consists of a charge-sensitive amplifier, voltage comparator, counter (shared by 16 pixels and implemented by cascading D flip-flops in each pixel), gated clock circuit, source follower circuit, and digital readout buffer circuit.

[Figure 1: see original paper] shows the overall chip architecture. The working principle of the chip is illustrated in [Figure 2: see original paper]. For energy measurement, when heavy ions strike a pixel unit, they generate numerous electron-hole pairs along the incident track. These charges are collected by the diode under the influence of the electric field [**?**, **?**] and then received, amplified, and converted into voltage signals by the charge-sensitive preamplifier (CSA). To reduce pixel area, this design replaces the peak holder by increasing the CSA' s decay time.

For time measurement, after charge collection and conversion to a voltage signal by the CSA, a comparator discriminates the signal to produce a transition signal. This transition edge triggers a counter to start timing until a control signal ends the timing period, thereby obtaining the particle' s Time of Arrival (ToA).

Under normal operation, STOP is high at the beginning of each scanning period, with a narrow pulse appearing before the end of each scanning period. When a particle hits, the energy channel maintains the voltage signal generated by the particle incidence under the CSA's long decay time. Simultaneously, the counter times during the period when the comparator output is high. When STOP goes low, the gated clock suspends the clock input to the counter, which stops timing and holds the time information until the CSA decay ends and COMP_{OUT} returns to low, at which point the counter automatically resets.

[Figure 2: see original paper] shows the measurement method for particle arrival time. Based on the time information output by the counter, the arrival time is calculated considering the STOP signal' s falling edge time, the counter' s output time information, and the comparator' s discrimination time error.

3.1 Charge-Sensitive Amplifier Design

The CSA is a commonly used preamplifier in high-resolution spectroscopy measurement systems, offering advantages of stable gain and low noise [**?**]. The front-end amplifier in this readout circuit adopts the CSA topology shown in [Figure 3: see original paper], where an NMOS transistor serves as the feedback resistor. The feedback resistance can be controlled by adjusting the gate voltage of this NMOS transistor. This design increases the CSA' s decay time by regulating the feedback resistor’ s dimensions and gate voltage to maintain the voltage signal, thereby replacing the peak holder.

The CSA amplifier employs a folded cascode structure, as shown in [Figure 4: see original paper], which provides a large output dynamic range. Since the charge-sensitive amplifier uses negative feedback, zero-pole simulation was performed. The simulation results in [Figure 5: see original paper] show that the charge-sensitive amplifier achieves an open-loop gain of 67 dB with a phase margin of 86°, indicating good stability.

Under input charges of 0.1-10 ke$^-$, the output amplitude exhibits a clear linear relationship with the input charge, as shown in [Figure 6: see original paper]. The slope indicates that the CSA’ s conversion gain exceeds 99 V/e$^-$.

Assuming the total parasitic capacitance at the CSA input is C_d, the equivalent input capacitance of this charge-sensitive amplifier based on the structure shown in [Figure 3: see original paper] is given by the standard CSA relationship. When the amplifier gain is sufficiently high, the CSA output voltage yields a gain that approximately equals the reciprocal of the feedback capacitance and is unaffected by the parasitic capacitance of the charge-sensitive device. To achieve large charge conversion gain while avoiding output saturation, the feedback capacitance in this CSA design is set to 1.3 fF. In the layout, interdigitated capacitors are formed using two metal layers and shielded with multiple metal layers to ensure capacitance accuracy and consistency across the pixel array.

When the substrate voltage changes due to body effects, the threshold voltage of the MOS transistor affects its equivalent resistance, and this variation is nonlinear with substrate bias. Therefore, the threshold voltage of MOS transistors under different substrate biases must be characterized [?]. By externally adjusting the gate voltage of the feedback NMOS transistor, resistance variations caused by threshold voltage changes can be compensated. Under 1 ke$^-$ input, to ensure the CSA maintains approximately 70% of its amplitude after 100 s, the gate control voltage of the CSA reset transistor was adjusted for different substrate biases, with results shown in .

shows the CSA decay parameters under different substrate bias and gate control voltages. In practice, this CSA design can adjust the decay time over a wider range by regulating the feedback transistor’ s gate voltage according to actual requirements. Taking the case of SUB at 0 V with 1 ke$^-$ analog input as an example, the CSA operating parameters are shown in .

presents the CSA operating parameters: energy resolution of 18 e$^-$, charge conversion gain of 99 V/e$^-$, decay time range of 7 s-5 ms, and amplitude decay to 70% in 1.9 s/670 s.

3.2 Voltage Comparator Design

Voltage comparators are typically used to compare two voltage signals. When the CSA output exceeds the comparator threshold, the comparator flips to high, and this transition edge contains the particle incidence time information. The comparator circuit design, shown in [Figure 7: see original paper], employs a two-stage operational amplifier structure. The reference voltage COMP_{VREF} is provided externally and can be adjusted to change the comparator threshold.

The comparator threshold in this design is determined based on the CSA reference voltage and minimum input charge. With the CSA reference voltage at 1.6 V and charge measurement range above 100 e^{-}, COMP_{VREF} is set to 1.61 V, which introduces some TimeWalk [?]. Post-layout simulation of the pixel unit' s TimeWalk was performed. Since most charge collected by the diode exceeds 500 e^{-} [?], TimeWalk was tested for different charge inputs ranging from 0.5-10 ke^{-}, with results shown in .

shows the comparator TimeWalk parameters for different charge inputs. Considering this design' s charge input range of 0.1-10 ke^{-}, the comparator reference voltage can be adjusted from 1.61-2.6 V. With increased threshold voltage, TimeWalk was tested for minimum input charges of 300 e^{-}, 500 e^{-}, and 1 ke^{-}, with results presented in .

demonstrates that TimeWalk varies under different reference voltages. Higher reference voltage (higher input charge threshold) results in larger TimeWalk. Setting the reference voltage to 1.61 V minimizes TimeWalk.

3.3 Counter Design

The counter consists of multiple D flip-flops cascaded together, as shown in [Figure 8: see original paper]. Each D flip-flop can record the state of one binary bit. This design shares one 16-bit DFF counter among 16 pixels using a 40 MHz clock, achieving a time resolution of 25 ns.

The RST signal controls the counter' s start and stop timing. In this design, COMP_{OUT} is connected to the counter' s RST. When COMP_{OUT} outputs high, the counter begins timing at the rising edge of clock CLK. If CLK is gated off, the counter holds its timing value. When COMP_{OUT} goes low, the timer resets to zero.

3.4 Gated Clock Circuit Design

This design must ensure that timing information is held before automatic system reset, which can be achieved by pausing the clock input to the counter. In CMOS circuits, a gated clock [?] is a clock signal enabled or disabled by a control signal. Gated clocks reduce dynamic power consumption and electromagnetic interference, which is particularly important in low-power designs. In this design, the gated clock is used to pause the clock signal to maintain the asynchronous counter' s output.

The gated clock circuit structure is shown in [Figure 9: see original paper]. To implement timing that starts at the comparator output COMP_{OUT} rising edge, stops and holds at the STOP falling edge, and ensures every particle incidence event can be read out, this design must maintain counter information until COMP_{OUT} returns low. This functionality is implemented using two AND gates and one DFF to control the counter' s clock input. Except for the externally controlled STOP signal, all other signals are generated internally. The KEEP signal is controlled by both COMP_{OUT} and STOP, with its structure shown in [Figure 10: see original paper]. The comparator output passes through an inverter to the DFF, with the STOP signal connected to the DFF' s CLK input. Therefore, when STOP rises high, the output KEEP signal becomes the inverted comparator signal. The complete timing sequence of the gated clock circuit is shown in [Figure 11: see original paper].

4 Nupix-H2- Complete Functional Verification

To reduce crosstalk between digital and analog signals, this design separates the analog and digital modules of each pixel unit in the layout, as shown in [Figure 12: see original paper]. In the 1 × 16 test pixel array layout, the gated clock module is on the far left, followed by pixels 0–15. Each pixel unit has analog circuitry on the left and digital circuitry on the right, separated by approximately 1.2 m. Notably, since this design shares one counter among 16 pixels, the 16 DFFs in the 16-bit counter are distributed across the 16 pixels and interconnected to implement the counter function, which reduces pixel area and average power consumption.

The test array uses Rolling Shutter [?] for readout. Each pixel has its own ROW_{SEL} and first-stage source follower, while each column shares a COL_{SEL} and source follower. During testing, starting from the first row, column select switches are sequentially opened to output pixel unit information column by column.

Assuming the pixel unit in the first row and first column is hit by a particle, [Figure 13: see original paper] shows the timing diagram for this pixel over three scanning periods. In the first scanning period, no particle hits, so the energy channel A_E_{OUT}[0] and timing channel A_T_{OUT} show no signal output. After particle incidence, COMP_{OUT} outputs high. Before the end of this period, the STOP signal is pulled low to preserve the counter timing information. At the beginning of the second scanning period, the KEEP signal maintains the timing information. When row and column switches open, A_E_{OUT}[0] and A_T_{OUT} output the particle' s energy and timing information. At the start of the third scanning period, both channels can still output the previous particle hit information until the output voltage falls below the flip threshold, when the system automatically resets and waits for the next particle hit.

Notably, the Rolling Shutter readout scheme introduces some dead time [?]. If particle incidence occurs after row/column scanning, the hit information may not be output. However, this design saves each particle hit information at the end of the current row/column scanning period and reads it out during the next scanning period, effectively avoiding dead time caused by the Rolling Shutter structure. Although this design employs a CSA with a long decay time, the resulting dead time can be neglected considering the low event rate of particle hits on the sensor in practical applications.

4.1 Pixel Array Energy and Time Channel Functional Verification

With the CSA reference voltage set to 1.6 V and comparator reference voltage to 1.61 V, post-layout simulation was performed on all 16 energy channels simultaneously at 10 s. Pixels 0–3 received 1 ke$^-$ analog charge input, pixels 4–7 received 1.5 ke$^-$, pixels 8–11 received 2 ke$^-$, and pixels 12–15 received 2.5 ke$^-$. The energy channel simulation results are shown in . Under simultaneous 16-channel analog input, the energy channels operate normally. Due to crosstalk between signals and larger parasitic capacitance in the pixel array, the CSA' s charge conversion gain decreases. The results show that under 1 ke$^-$ input, CSA_{OUT} voltage rise is ~86 mV, corresponding to a charge conversion gain of ~86 V/e$^-$. After three stages of source follower circuits, A_E_{OUT} voltage rise is ~46 mV, yielding an energy channel charge conversion gain of ~46 V/e$^-$. Complete CSA decay for 1 ke$^-$ input requires approximately 500 s.

Scanning the energy channel output under 0.1–10 ke$^-$ charge input yields the linear output curve shown in [Figure 14: see original paper]. The post-layout simulation of the 16 energy channels demonstrates a linear relationship between output and input charge. However, due to crosstalk from 16 pixels operating simultaneously, the energy resolution is ~5%.

Transient noise simulation of the complete circuit yields the Equivalent Noise Charge (ENC) results shown in [Figure 15: see original paper]. With all 16 energy channels operating simultaneously, the circuit array' s ENC is less than 30 e$^-$, meeting expectations.

Post-layout power consumption testing of the test array shows a static current of ~1.34 A per pixel and dynamic current of ~3.88 A. With 1 ke$^-$ charge input hitting pixel 0 at 10 s and pixel 15 at 550 s, and 10 e$^-$ hitting pixel 7 at 1.1 ms, the simulation results are shown in [Figure 16: see original paper]. Both charge inputs at 10 s and 550 s trigger normal counter timing, while the 10 e$^-$ input at 1.1 ms does not reach the measurement threshold, resulting in zero time channel output. At 10 s, after the first charge input, both COMP_{OUT} and STOP are high, and the timing channel begins working. The timing result is the analog signal level output, converted to digital where high level represents digital "1"and low level represents "0" . The timing information shown is 0000111001011101b. At approximately 420 s, the CSA output falls below the COMP_{OUT} flip threshold, COMP_{OUT} goes low, the counter information clears, and the system automatically resets.

4.2 Pixel Array Mixed-Signal Simulation Verification

Since the test array has 16 pixels scanned at 40 MHz clock frequency, one scanning period is set to 400 ns. Row switches open for 400 ns (25 ns × 16), and 16 column switches open sequentially for 25 ns each. The STOP signal goes high at the beginning of each scanning period to record particle hit information and goes low before the period ends to preserve the hit information. When the START signal goes high, if the SPEAK signal is also high, the system enters scanning readout state and begins readout in Rolling Shutter mode. If SPEAK is pulled low, scanning stops at the current state. MARKER indicates the start of each scanning readout cycle.

[Figure 17: see original paper] shows the mixed-signal simulation results for six scanning periods. No charge input occurs during the first two periods. In the third period, all 16 pixels receive simultaneous 1 ke$^-$ analog input. The energy channel output voltage information shows A_E_{OUT}<0-15> at 1.153 V. Since the baseline voltage without charge input is 1.11 V, the actual energy channel output voltage is 43 mV, corresponding to a charge conversion gain of 43 V/e$^-$. Examining the timing channel information, the first output is inaccurate due to charge injection from comparator flipping. To avoid timing errors, the timing information after the second scanning period following charge input must be observed. The true timing information is 000000001010b, corresponding to a counting time T_{CNT} of 250 ns. With STOP signal set at 20313 ns and considering ~50 ns TimeWalk, the particle arrival time T_{oA} = T_{STOP} - T_{CNT} - T_{TimeWalk}   20013 ns. The actual particle arrival time is 20000 ns, yielding an error of ~13 ns, which satisfies the 25 ns time resolution requirement.

5 Conclusion

This paper presents the design of a test array for a monolithic active pixel sensor chip capable of detecting particle hit timing information, hit pixel position, and corresponding energy amplitude. The pixel test array comprises 16 pixel units with individual pixel area of 22 m × 22 m, achieving ENC less than 30 e$^-$, energy resolution of ~5%, and time resolution within 25 ns. Simulation of the chip test array confirms that all functions and performance metrics meet design requirements. The next step will involve completing the 128 × 128 pixel array design for Nupix-H2 and improving the circuit’ s energy resolution.

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Note: Figure translations are in progress. See original paper for figures.