

Field Programmable Droplets Array: An Active-matrix digital microfluidics platform for field programmable high-throughput digitalized liquid handling

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Abstract

Digital liquid sample handling is an enabling tool for cutting-edge lifesciences research. Similar to Field Programmable Gate Arrays (FPGA) in Integrated Circuits, we present here an active-matrix thin-film electronicsbased digital microfluidics system, which will be henceforth referred to as Field Programmable Droplets Arrays (FPDA). The system contains 256×256 pixels in an active area of 10.65 cm^2 , which is capable of manipulating thousands of individually addressable liquid droplets simultaneously. By leveraging a customised TFT-based circuit design solution, it becomes possible to programmatically manipulate droplets at the pixel level. The minimum achievable droplet volume is around 0.5 nl , which is two orders of magnitude smaller than the state-of-the-art reported¹. The movement of droplets can be either pre-programmed or controlled in real-time. The FPDA system shows great potential of the ubiquitous thin-film electronics technology in digital liquid handling. These efforts will make it possible to create a true programmable lab-on-a-chip device to enable great advances in life science research.

Full Text

Preamble

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Field Programmable Droplets Array: An Active-Matrix Digital Microfluidics Platform for Field Programmable High-Throughput Digitalized Liquid Handling

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Digital liquid sample handling is an enabling tool for cutting-edge life sciences research. Similar to Field Programmable Gate Arrays (FPGA) in integrated circuits, we present here an active-matrix thin-film electronics-based digital microfluidics system, which will henceforth be referred to as Field Programmable Droplets Arrays (FPDA). The system contains 256×256 pixels in an active area of 10.65 cm^2 , capable of manipulating thousands of individually addressable liquid droplets simultaneously. By leveraging a customized TFT-based circuit design solution, it becomes possible to programmatically manipulate droplets at the pixel level. The minimum achievable droplet volume is around 0.5 nL , which is two orders of magnitude smaller than the state-of-the-art reported¹. The movement of droplets can be either pre-programmed or controlled in real-time. The FPDA system demonstrates great potential for ubiquitous thin-film electronics technology in digital liquid handling. These efforts will make it possible to create a true programmable lab-on-a-chip device to enable great advances in life science research.

For decades, Very Large-Scale Integrated Circuits (VLSI) have greatly changed people's lives and paved the way to the digital era^{2,3}. There are two broad categories of VLSI: Application Specific Integrated Circuits (ASIC) and Field Programmable Gate Arrays (FPGA)⁴. ASICs are customized designs targeted to solve specific tasks, while FPGAs can be reprogrammed to meet desired application specifications or functionality requirements⁵. Due to their programmability and flexibility, FPGAs tend to be preferred for many different applications and markets.

Recently, numerous Lab-on-a-Chip (LOC) platforms have emerged along with innovative technologies for various application areas⁶⁻⁸. LOCs can also be divided into two broad categories. The first is the traditional microfluidics chip based on custom micro-channel designs, which will be referred to as integrated fluidic circuits (IFC)⁹. IFCs have been in continuous development for more than 20 years towards not only LOC, but also the micro-Total Analysis System (TAS)¹⁰. However, several unavoidable problems restrict their practical application. For instance, most IFCs require a micro-pump for driving the liquid, which greatly increases the size and complexity of the platform. The liquid in IFCs is

usually continuous, or even if discrete droplets can be generated, the droplets are not individually addressable. The micro-channels or micro-structures in IFCs have low yield, increasing fabrication cost and hindering commercial mass production^{11–13}.

It is therefore necessary to build a new type of LOC that is not subject to these limitations. Firstly, overcoming the one-dimensional restriction of micro-channels is necessary to allow free movement of droplets on a two-dimensional planar surface. To solve this, droplet manipulation is electrically driven using a method called electrowetting-on-dielectric (EWOD)¹⁴. EWOD is a physical phenomenon that allows manipulation of liquid droplets by applying an electric field to change the surface wettability¹⁵. Therefore, by utilizing an electrode array, water droplets can be manipulated freely on the electrode array surface¹⁶. Due to its programmable nature, much like FPGA, it will be referred to as Field Programmable micro-Droplet Array (FPDA).

IFCs usually involve the use of lithography to create micro-channels and reservoirs on a substrate, which is then bonded to another substrate either thermally or chemically to create a watertight seal. In comparison, FPDA has no prefabricated micro-channels or micro-structures, and each droplet on the FPDA can be addressed and controlled independently, thus achieving more flexible and complex droplet operations¹⁷. Additionally, the fabrication of FPDAs is based on standard thin-film processes, which are more mature and precise, resulting in greater mass market production scalability^{18,19}. This makes FPDAs a more attractive solution for a wider range of applications beyond the capability of conventional IFCs.

Active-Matrix FPDA

Most existing FPDA systems are based on passive electrode arrays, in which each electrode connects to peripheral electronics directly. Due to space limitations of driving signals and layout wiring, scalability issues greatly restrict the scale of passive-matrix electrode arrays. Active matrix (AM) technology provides a perfect solution for addressing this issue²⁰. In an AM array, pixel circuits contain electronic switches and capacitors to store a logic voltage. Each pixel can be addressed by row and column signal scanning, thus enabling independent pixel control and scalability of the AM array. An additional benefit of AM technology is that an array sized N (rows) \times M (columns) is addressable by only $N + M$ control signals. All addressable pixels can be programmed to provide sequenced patterns for liquid droplets on-chip to realize a FPDA for lab-on-a-chip applications (Supplementary Section 1).

Depending on the basic micro switch used, there are two methods to realize FPDA: the first is TFT, while the other is based on complementary metal oxide semiconductor (CMOS). TFT-based FPDAs are generally fabricated on glass substrate, while CMOS-based chips are fabricated on silicon wafer, thus their fabrication costs are not in the same order of magnitude. In addition,

TFT-based FPDA chips possess the ability for large-area fabrication processes and high optical transparency, which cannot be achieved on traditional silicon wafers^{21–23}. These benefits indicate that a TFT-based device is more suitable for FPDA.

[Figure 1: see original paper] Design of an active-matrix digital microfluidics based FPDA system. a, Cross-section view; b, 3D view; c, photograph of a 256 \times 256 pixels FPDA; d, picture of a part of the array; e, picture of the GOA circuits; f, picture of the MUX circuits.

A full view of the FPDA chip is shown in Fig. 1f, and details of decomposed parts can be seen in Fig. 1c, 1d & 1e. The layout of the FPDA chip can be seen in Supplementary Section 2. As mentioned before, AM technology is an ideal method for solving scalability issues present in PM matrices. Different functional circuits are designed to realize a massive-scale active-matrix electrode array by further reducing row and column driving signals. In an AM matrix, each pixel can be individually addressed by the row and column scanning method, in which row scan signals are transmitted line by line, making it possible to use a shift register for generating and transmitting the row scan signals. The shift register circuits are also referred to as gate on array (GOA) and located on one side of the electrode array (shown in Fig. 1d).

The GOA circuits can generate several hundreds of driving signals serially, while the GOA itself needs only 4 driving signals, thus significantly reducing the number of external row driving signals. The column data outputs are in parallel, and another circuit is designed to reduce column driving signals instead of serial GOA circuits. The circuit is simple and effective, where several TFTs control a column data signal into the pixel array. By turning each TFT device on in sequence, one data signal can be divided into several parallel driving signals. Here, 4 TFTs are used to control one data signal, so the number of column-driving signals has been reduced by nearly 4 times. With these modifications, it is possible to address 65,536 pixels using fewer than 80 driving signals (Supplementary Section 3).

Thin-Film Transistor Device Structure Optimization

To realize large-area droplet manipulation, a well-designed driving strategy is necessary, which requires the design of TFT device and pixel circuit. The driving voltage requirements in FPDA differ from other applications, particularly regarding high voltage transmission and pixel voltage stability. We compared and simulated the TFT device and pixel circuit of the FPDA chip, and Fig. 2a-2i shows the TCAD simulation results of channel temperature distribution and voltage drop across different TFT devices. Fig. 2a shows the 3D structure of the normal bottom-gate bottom-contact (BGBC) TFT device, which is the common structure of amorphous silicon. The channel width/length (W/L) of the BGBC TFT is 20 μm / 6 μm . When a high voltage up to 50 V is applied to the gate electrode and 40 V to the drain electrode, a drain current of around

100 A is produced. High drain current stress causes the self-heating effect of the TFT device, leading to performance degradation such as threshold voltage (V_{th}) shift, channel current drop, transconductance distortion, etc. Therefore, to improve high-voltage performance of TFT devices, the conventional method is to place a high-resistance area between the drain and channel, namely drain-offset²⁴. Fig. 2b shows a typical structure of drain-offset TFT, where the gate electrode does not overlap with the drain electrode. The channel width of the offset TFT is 20 μm , with an offset length of 3 μm and a channel length of 6 μm . The drain-offset area could divide the high drain voltage applied to the channel, thus reducing the high drain current transferred in the channel. The disadvantage of a drain-offset TFT device is that the resistance of the offset area is very large, which increases the overall gate-on resistance and reduces the total channel on-current.

To address this, a new TFT structure was designed, as shown in Fig. 2c & 2f, which will henceforth be referred to as the diamond TFT structure. The diamond TFT comprises two channels separated by a floating electrode. Both channels have different widths but equal length of 6 μm . The width of the innermost channel is 14 μm , whereas the width of the outermost channel is 30 μm . Two channels in series can withstand the high voltages applied on the drain electrode, thus reducing the transverse electric field strength. Compared to traditional single-channel TFTs, the floating electrode in diamond TFT could form a balanced electric field inside the channel, improving device stability.

Fig. 2g-2i show the temperature-distribution simulation of the three TFT devices. Due to different dimensions of the three devices, the device sizes were normalized. When the same voltage is applied to all three types of TFT devices, the channel temperature of the conventional single-channel device is the highest, and the channel temperature of diamond devices is between the offset device and single-channel device. Fig. 2j-2m show the potential distribution simulation of the three TFT devices. The channel of offset TFT serially connected to a high-resistance region results in a significant voltage drop in that region. The diamond TFT also has a voltage drop in the inner channel, while the current transmission capability is better than the offset TFT device. To further compare characteristic differences of the three TFT devices, the output curve of the TFT device was measured and the equivalent resistance was calculated. As shown in Fig. 2n, when the gate is open, the channel resistance of diamond TFT is smaller than the offset TFT and normal TFT, meaning diamond TFT has better current transmission characteristics. Additionally, diamond TFT has better positive bias stress (PBS) stability, as shown in Fig. 2p & 2q. After 10k seconds, the threshold voltage (V_{th}) shift of diamond TFT is less than 10V, while other TFTs exceed 10V (Supplementary Section 4).

[Figure 2: see original paper] Optimization of the TFT device in FPDA. a-c, Stereogram of temperature distribution in normal TFT, offset TFT and diamond TFT; d-f, cross-section view of the three TFTs; g-i, temperature curve with TFT length of the three TFTs; j-m, potential variation with TFT position

in the three TFTs; n, equivalent resistance of different TFTs under different gate voltages; p, threshold voltage stability of different TFTs under gate positive bias stress; q, on current stability of the three TFTs under different gate positive bias stress time.

Pixel Circuit Design and Simulation

Based on the improved TFT device design, the FPDA chips were optimized for pixel circuit operation. Presently, there are mainly two types of pixel circuits reported: the 1T1C²⁰ and the SRAM²⁵. Generally, the 1T1C circuit is a simple passive circuit (shown in Fig. 3a), while SRAM is a complicated active circuit. In the 1T1C circuit, the pixel electrode is driven by charge stored in the capacitor. As a capacitor is a passive component, the stored charge will gradually leak out from the TFT and pixel electrode. Under circumstances of high temperature or light exposure, the leakage current will rise by several orders of magnitude. In this case, the leakage rate of stored charge will accelerate, greatly reducing pixel voltage and droplet driving force. To avoid this, a power signal needs to be introduced into the pixel circuit to realize active driving.

SRAM is an ideal active circuit, the basic structure of which is bistable. The voltage of pixel electrodes driven by SRAM can remain constant, regardless of leakage current. Thus, the driving force on droplets can also be maintained continuously. So far only one kind of SRAM circuit has been reported, designed by Sharp Life Science (EU) Ltd²⁵. The downside of the reported SRAM circuit is that it requires about 14 TFTs. Increasing the number of TFT devices in a pixel circuit results in a pixel layout size of 210 μm , making it difficult to reduce the layout space further. More TFT devices in the pixel circuit occupy larger layout space, limiting applications such as single-cell sorting and large-area FPDA chips.

Considering both driving ability and layout space, we designed a pixel circuit with only 4 TFTs and a capacitor (named 4T1C) based on the commercialized amorphous silicon (a-Si) process. As shown in Fig. 3b, a power source VCC has been introduced into the pixel circuit to maintain driving voltage. The pixel size is 127.5 μm (shown in Fig. 3c & 3d), which is much smaller than the reported SRAM circuit size of 210 μm and the reported 1T1C circuit size of 1000 μm ²⁰. Fig. 3e & 3f simulated the pixel voltage of 1T1C circuit and 4T1C circuit. As the 4T1C circuit introduces a VCC power to drive the pixel electrode, the charge stored in the capacitor only needs to keep the gate voltage stable. Compared with the 1T1C circuit, the 4T1C design reduces the leakage path of capacitor-stored charge. Thus, the gate voltage of driver TFT (T1) tends to remain stable, enhancing pixel voltage driving ability.

[Figure 3: see original paper] FPDA pixel circuit design. a, a 1T1C pixel circuit; b, a 4T1C pixel circuit; c, the layout of the 4T1C pixel circuit; d, a photomicrograph of the 4T1C circuit; e, pixel electrode voltage simulation of a 1T1C and a 4T1C circuit; f, pixel electrode voltage charge details of the 1T1C and

the 4T1C circuit.

When fabricating the FPDA chip, in addition to TFT device and array circuit design, several items must be carefully considered. Table 1 summarizes the recommended specifications for different components of the FPDA chip, including fabrication process parameters for the backplane glass substrate and the cover ITO glass. These parameters were obtained through continuous optimization and iteration of FPDA chip design and have been verified experimentally. In this work, we followed the recommended specifications to ensure FPDA chip performance.

Summary of the recommended specifications to fabricate the FPDA.

Components	Structure Items	Recommended Specifications	This work
Metal	Sheet resistance	\$ \$1E-6A	1E-5A
		\$ \$1E-10A	5E-11A
		\$ \$2V/dec	1~2V/dec
		\$ $0.5cm^{2}/(V \cdot S) 0.55cm^{2} \$/ (V \cdot S)$	
Dielectric	Breakdown strength	\$ \$0.5Ω/ \$ \$2MV/cm	0.4Ω/ 2~3MV/cm
	Equal height area ratio	\$ \$5%	-
Substrate	Surface height difference	gap	-
	X/Y tolerance	\$ \$50nm	30~40nm
	Z tolerance	\$ \$100Ω/	80Ω/
Hydrophobic Layer	Contact angle	\$ \$110°	-
	Rolling angle	-	-
Cover plate	Surface height difference	\$ \$50nm	30~40nm
	Sheet resistance	\$ \$100Ω/	80Ω/
	Inlet/outlet	\$ ±\$5%diam	\$ ±\$50um
	X/Y tolerance	\$ ±\$0.15mm	\$ ±\$0.15mm
	Z tolerance	\$ ±\$0.05mm	\$ ±\$0.04mm
Outline	Transmittance	-	-
	Diam tolerance	\$ ±\$50um	\$ ±\$50um
	Location tolerance	\$ ±\$0.15mm	\$ ±\$0.15mm
	X/Y tolerance	\$ ±\$0.12mm	\$ ±\$0.04mm
	Z tolerance	\$ ±\$0.04mm	-

Field Programmable Droplets Array for Concentration Gradient Generation

Traditional IFC microfluidics are generally based on physical micro-channels. In comparison, FPDA chips have no prefabricated micro-channels, thus the liquid manipulation process is quite different. On traditional IFC microfluidics platforms, droplets are generated by coordination of pumps and micro-channels. The flow path and volume of droplets on IFC microfluidics are commonly fixed and restricted, making it difficult to address and manipulate target droplets. However, with FPDA chips, each individual droplet is addressable and its volume can be controlled. The array scale of FPDA chips is much larger than that of traditional IFC microfluidics. The massive pixels in the AM array pave the way for high-throughput and versatile reaction of liquid droplets, providing the ability to split, sort, and merge different sizes of droplets freely and dynamically. These liquid operations are routine on FPDA chips, while being almost impossible using traditional microfluidic chips.

[Figure 4: see original paper] Virtual channel microfluidics and droplet fluorescence intensity gradient. a, virtual channel of DI water and CQDs fluorescent solution in different lengths; b-d, mixing of DI water and CQDs fluorescent solution; e, bright field and fluorescence images of fluorescent solution with different concentration gradients; f, intensity values extracted from the fluorescence image; g, stereoscopic image of fluorescent solution with different concentration gradients.

To further showcase application scenarios of FPDA chips, an experiment was designed to realize different concentration gradients of carbon quantum dots (CQDs) fluorescent solution. As shown in Fig. 4a, liquid droplets were generated in various pixel sizes, appearing as if arranged by virtual channels. The droplets were then mixed by moving them back and forth to evenly mix the reagent (shown in Fig. 4b-4d). Fig. 4e & 4f show bright field and fluorescence images of fluorescent solution with different concentration gradients. The fluorescence intensity values of different droplets have also been extracted in Fig. 4g & 4h. It can be seen that the 20 droplets have relatively different concentrations from each other, indicating that the AM-FPDA chip can realize high-throughput concentration gradients using virtual channels.

Concentration Gradient Generation

To realize the best control precision and highest array usage efficiency of FPDA chips, it is necessary that a single pixel can drive a single droplet independently. The one-to-two droplets generation method has been applied to generate massive individual droplets in a short time. The bisection generation principle is simple and effective: one droplet subdivides into two, then two droplets divide into four, and so on. In this way, the number of single droplets can be increased exponentially (Supplementary Section 5). Fig. 5a-5k shows the droplet generation process using the bisection method, with a time interval of about 0.5s for

each step. Based on the bisection generation method, one droplet can be continuously divided into two. Under control of the AM electrode array, thousands of single droplets can be obtained in about 80 seconds. As the pixel number of the FPDA chip is 65,536, it is capable of generating more than four thousand droplet arrays (shown in Fig. 5k).

The droplet manipulation principle of FPDA chips is based on EWOD, which is sensitive to driving signals and interface state. In the bisection process, droplet volume keeps halving while pixel pitch remains invariant. Therefore, the droplet gradually approaches the limit size that cannot be bisected. Fig. 5m illustrates the generation percentage of droplets of different sizes. Size was defined by the number of pixels occupied by the droplet. When droplet size is larger than 2×2 , the success rate of droplet generation is close to 100%. When droplet size is smaller than 2×2 , the success rate reduces to about 90%. The single-pixel droplet is the most difficult to generate, with a typical success rate of about 70%. There is a limit to the minimum droplet size that can be generated by FPDA, related to the ratio of gap to droplet size. When generating a single-pixel droplet, the droplet size approaches the splitting limit, and the EWOD force is unable to break through the critical value of surface tension, leading to failure of single droplet generation.

[Figure 5: see original paper] High-throughput droplets array generation process and generation percentage. a-k, the generation step time of different droplet sizes; m, generation success percentage of different droplet sizes.

Conclusions

In conclusion, we have demonstrated a robust and powerful tool for generating and manipulating micro-droplets, namely the FPDA platform. The FPDA chip possesses 65,536 pixels and can realize high-throughput droplet generation and manipulation at the single-pixel level. All droplets can be addressed and manipulated independently, with a minimum droplet volume of about 0.5 nL. The FPDA platform has potential to revolutionize applications in point-of-care diagnostics, drug development, and environmental monitoring. The high accuracy and real-time capabilities of FPDA chips offer greater sensitivity and specificity for detection and analysis of biomolecules and cells. Integration of multiple functionalities on a single chip could lead to new miniaturized analytical tools that are more accurate, efficient, and sensitive than current technologies. This work demonstrates the great application potential of TFT technology in FPDA platforms, creating new breakthroughs for lab-on-a-chip systems. Based on the FPDA chip, the droplet analysis system could be further miniaturized with higher throughput. Our study serves as a foundation for future research aiming to optimize droplet manipulation techniques and unlock the full potential of FPDA-based microfluidic devices.

Methods

Carbon Quantum Dots solutions were purchased from Suzhou Xingshuo Nanotech Co., Ltd. (Suzhou, P.R. China), with a concentration of 10 mg/mL, extraction wavelength of 480 nm, and photoluminescent wavelength of 514 nm.

FPDA device fabrication. We designed and fabricated the FPDA device. The fabrication process of TFT-based FPDA is similar to the backplane of flat panel displays, both of which are fabricated by thin-film electronic technology and photolithography processes. The structure of the FPDA device is shown in Fig. 1a & 1b. The amorphous silicon TFT array was fabricated on a glass substrate, with an electrowetting dielectric layer (300 nm SiNx) and a hydrophobic layer deposited on top of the TFT array. A plastic spacer (not shown in Fig. 1b) was used to define the gap (30 μ m) between the bottom glass substrate and the ITO-coated cover glass plate. The side of the ITO layer facing the bottom was also coated with a thin hydrophobic material layer. The conductive ITO was constantly connected to system ground, forming a direct electric field across the gap when a corresponding pixel at the bottom is selected. Surrounding medium oil was used to suppress liquid droplet evaporation and enhance droplet mobility.

Electronics system. The FPDA device features an active-matrix array of 256 \times 256 elements, totaling 65,536 addressable pixel electrodes. We use a MUX to separate 1 column signal into 4 columns. The MUX contains 4 TFTs controlling each TFT to open in sequence. Row signals are generated by the described GOA circuits. The GOA circuits require 4 driver signals: CK, CKB, STV, and RST. CK and CKB are two inversion clock signals; STV is a stimulus signal to activate the GOA circuits; RST is a reset signal to reset all output signals of the GOA circuits. The FPDA needs 64 column signals and 4 GOA signals. We use a DC-DC power supply to provide voltage for the FPDA platform, and an STM32 embedded system to control the driving signals.

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Author Contributions

D.W., K.J., and H.M. conceived the concept and experiments. D.W., K.J., C.H., M.D., and S.S. carried out the experiments. D.W., Y.B., J.L., S.H., and J.Y. collected and analyzed the data. D.W., K.J., A.N., and H.M. wrote the manuscript, and all authors reviewed and commented on the manuscript.

Competing Interests

Patents based on this research have been submitted.

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