Design and Development of a Multi-channel, Bipolar QDC Front-end Electronics System for SiPM Detectors

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Abstract

With the development of silicon photomultiplier (SiPM) technology, front-end electronics for SiPM signal processing are highly sought after in various fields. This paper implements a compact 64-channel front-end electronics (FEE) system by constructing and developing a field-programmable gate array-based charge-to-digital converter (FPGA-QDC). The FEE consists of an analog board and an FPGA board. The analog board comprises commercial amplifiers, resistors, and capacitors. The FPGA board is composed of a low-cost FPGA. This paper evaluates the electronic performance of the FEE in terms of noise, linearity, and uniformity. The readout capability of the FEE for SiPM-based detectors is verified by designing a positron emission tomography (PET) detector with three different readout configurations. The PET detector consists of a 15$×$15 LYSO crystal array directly coupled to an SiPM array detector. Experimental results demonstrate that the FEE can process bipolar charge signals from SiPM detectors. Furthermore, under dual-ended readout of the LYSO crystal array irradiated by a Na-22 source, it shows good energy resolution for 511-keV gamma photons. Overall, the FPGA-QDC-based FEE is promising for application in various SiPM-based radiation detectors.

Full Text

Design and Development of Multi-channel Front End Electronics Based on Dual-Polarity Charge-to-Digital Converter for SiPM Detector Applications

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Abstract

With the advancement of silicon photomultiplier (SiPM) technology, front-end electronics for SiPM signal processing have become highly sought after across various fields. This paper presents the development of a compact 64-channel front-end electronics (FEE) system implemented using field-programmable gate array-based charge-to-digital converter (FPGA-QDC) technology. The FEE system comprises an analog board and an FPGA board. The analog board incorporates commercial amplifiers, resistors, and capacitors, while the FPGA board utilizes a low-cost FPGA. The electronic performance of the FEE was evaluated in terms of noise, linearity, and uniformity. To validate the readout capability of the FEE for SiPM-based detectors, a positron emission tomography (PET) detector with three different readout configurations was designed. The PET detector consists of a 15 × 15 lutetium–yttrium oxyorthosilicate (LYSO) crystal array directly coupled to a SiPM array detector. Experimental results demonstrate that the FEE can successfully process dual-polarity charge signals from SiPM detectors and achieves good energy resolution for 511-keV gamma photons under dual-end readout when the LYSO crystal array is irradiated by a Na-22 source. Overall, the FPGA-QDC-based FEE shows promising potential for application in SiPM-based radiation detectors.

Keywords: readout electronics, charge measurement, radiation detector, silicon photomultiplier, field-programmable gate array

1 Introduction

Semiconductor-based detectors have been widely employed as radiation detectors across diverse fields, including astrophysics [**?**], medical imaging applications [**?**], and high-energy physics [**?**]. Recently, silicon photomultipliers (SiPMs) have emerged as a viable alternative to photomultiplier tubes, offering a high gain of approximately 10^6. SiPM performance remains stable in strong magnetic fields, and their bias supply requirements are decreasing (approximately 24 V). These advantages have positioned SiPMs as a new candidate for various experimental applications [**?**]. In nuclear medicine, SiPM-scintillator combinations are commonly utilized in PET detectors. Current SiPM technology enables PET detectors to achieve excellent performance in energy resolution, crystal discrimination, coincidence timing resolution, and depth of interaction. Furthermore, strip SiPMs have gained attention due to their precise timing and positioning capabilities [**?**].

Multiple approaches exist for reading signals from SiPM-based detectors. Traditional charge readout schemes for single-pixel SiPMs, including front-end electronics (FEE) based on signal integration and shaping [**?**] and data acquisition systems employing commercial analog-to-digital converters (ADC) [**?**], provide a rapid means of customizing signal processing electronics. However, these traditional methods face challenges when applied to multi-pixel SiPM arrays. Researchers have pursued various strategies to mitigate signal processing com-

plexity for SiPM arrays. On the detector side, multiplexing schemes with different ratios (8:1 and 16:1) have been developed [**?**], and both resistor-based and capacitor-based multiplexing circuits are now available [**?**]. On the electronics design side, two primary research paths have emerged for SiPM-based radiation detector readout. The first approach utilizes commercially available off-the-shelf discrete components and programmable chips. Numerous SiPM readout methods have been explored within this framework. For instance, the time-over-threshold (ToT) method is widely adopted due to its simple circuit structure [**?**], though ToT results suffer from poor precision due to intrinsic nonlinearity between deposited energy and pulse duration. Leveraging the abundant inputs/outputs (I/Os) and logic resources in field-programmable gate arrays (FPGAs), an FPGA-ADC scheme based on carry chain time-to-digital converter (TDC) has been developed to achieve compact multi-channel designs [**?**]. However, current FPGA-ADC implementations are limited to 25 MHz sampling frequency due to low dynamic range and poor resolution, requiring further development. The second research path involves application-specific integrated circuit (ASIC)-based readout methods, such as Triroc ASIC [**?**] and TOFPET2 ASIC [**?**]. While ASICs can deliver excellent performance, their development and validation demand high costs and long development cycles.

Strong motivations persist for developing cost-efficient, multi-channel, and easy-to-design FEE systems for SiPM-based detectors. Several studies have demonstrated potential for implementing highly integrated readout electronics [**?**]. Among these, the linear discharge scheme based on current low-cost FPGAs can achieve both good linearity and excellent timing performance [**?**]. This scheme provides a direct charge-to-digital converter (QDC). In the linear discharge approach, the analog portion requires only a capacitor, two resistors, and an operational amplifier (op amp), while the digital portion needs only an FPGA. The rich resources and I/Os in FPGAs make it feasible to handle multi-channel analog signals. The initial version of the linear discharge QDC could only process negative polarity signals, limiting its applications. In our previous study [**?**], we improved the linear discharge-based QDC to process both negative and positive charge signals (i.e., dual-polarity charge signals) through a simple modification, thereby extending the circuit' s application scope. Building upon this linear discharge QDC, we propose a compact, power-efficient, multi-channel FEE readout system for SiPM-based radiation detectors. The system consists of two parts: an analog board and an FPGA board. This paper provides a detailed description of the hardware design and presents evaluations of both electronics performance and detector applications using three different detector modules combined with LYSO and SiPM arrays.

2 Dual-polarity QDC based on linear discharge

The dual-polarity QDC based on the linear discharge scheme is illustrated in Fig. 1 [Figure 1: see original paper]. Implementing a linear discharge QDC requires both analog and digital circuits. The analog circuit comprises an op amp,

an integration capacitor, and two resistors (R_{discharge} and R_L), while the digital circuit requires only an FPGA. During quiescent operation, when no current pulse arrives from the SiPM detector, a 3-state buffer controlled by an FPGA module maintains a high-impedance state ('hz'), effectively disconnecting the resistors (R_{discharge} and R_L) from the FPGA. This configuration corresponds to a traditional charge-sensitive amplifier with a constant time constant of (R_{discharge} + R_L)C_f.

When the SiPM detector fires, the current pulse signal is first integrated on the feedback capacitor C_f, causing the op amp output voltage to increase. This voltage crosses a preset threshold V_{Thr}, triggering the LVDS (low voltage differential signaling) comparator and initiating the discharge process. For negative current pulse injection, V_{Thr} is set slightly above the op amp' s quiescent baseline, with the LVDS comparator output initially at logic '0'. The T port of the 3-state buffer is driven by the control module, producing a 'hz'output. The negative current pulse causes the LVDS comparator output to transition to logic '1' , prompting the control module to set the I port of the 3-state buffer to '1' . This applies a positive voltage V_{IO} (typically 2.5 V, the I/O bank voltage) to the FPGA discharging pin, generating a constant discharge current i_n(t) = V_{IO}/R_{discharge}. The discharge process continues until the op amp output voltage falls below V_{Thr} for the second time.

A voltage offset V_{offset} applied to the op amp's noninverting port adjusts the output baseline to ground. Theoretically, when V_{Thr} is set to ground, the pulse width T_{pulse} at the LVDS comparator output is strictly proportional to the total charge Q injected into the QDC circuit:

$$T_{pulse} = \frac{Q \cdot R_{discharge}}{V_{IO}}$$

If this pulse width is digitized by an FPGA counter driven by a system clock with frequency F_S, the digital code D is expressed as:

$$D = \text{floor}\left(\frac{T_{pulse}}{T_S}\right)$$

where the floor function returns the nearest integer for T_{pulse}/T_S.

For positive charge injection, the op amp generates a negative voltage pulse. Since the FPGA can only process signals above ground, a stage voltage V_{stage} (typically 2.5 V) is applied to pull up the op amp' s output baseline, making it manageable for the FPGA. In this case, V_{Thr} is set slightly below V_{stage}. During quiescence, the LVDS comparator output is logic '1' , and the T port of the 3-state buffer produces a high-impedance 'hz' output. When a positive current pulse arrives, charge integration on C_f lowers the op amp output voltage. Once this voltage falls below the preset V_{Thr}, the LVDS comparator output becomes logic '0' , causing the control module to

set the I port of the 3-state buffer to '0' and producing a ground output. This creates a reverse discharge current i_p(t) = V_{stage}/R_{discharge}. The subsequent process mirrors that for negative charges, though the discharge current directions differ for positive and negative charges. Notably, the leading edge of the discharge pulse in the linear discharge scheme marks event arrival, enabling simultaneous charge and timing measurements.

3 Hardware design

A stacked configuration was designed to achieve a compact FEE system, as shown in Fig. 2 [Figure 2: see original paper]. In this multi-channel FEE, analog and digital circuits are implemented on separate analog and FPGA boards, respectively.

3.1 Analog board

The analog board integrates analog circuits for dual-polarity QDC based on linear discharge, four 30-pin connectors (FH12 series, Samtec), and two 100-pin high-density connectors (ST4 series, Samtec). The 64 charge signals are organized into four groups of 16 signals each, with each group connected to one FH12 connector. Two ST4 series connectors facilitate board-to-board interconnection with the FPGA board. In these connectors, op amp outputs are referenced to analog ground, while discharging signals are referenced to digital ground.

The dual-polarity QDC analog circuit comprises 16 high-performance quad amplifiers, along with resistors and capacitors to implement the linear discharge circuits. At each op amp' s noninverting port, V_{stage} and V_{offset} are selectable to enable measurement of negative and positive charges, respectively. To enhance flexibility, an optional coupling capacitor C_0 is included for each channel; in direct coupling mode, this capacitor can be replaced by a resistor. All components are assembled on a 12-layer printed circuit board measuring 70 $\times$ 70 mm^2, as shown in Fig. 3 [Figure 3: see original paper]. This implementation yields an average area of 0.77 cm^2 per channel for the linear discharge-based QDC. During normal operation, a 5-V power supply (2231A-30-3, Tektronix) powers the analog board, drawing 0.310 A and resulting in an average power dissipation of 24.2 mW per channel.

3.2 FPGA board

The FPGA board centers on a low-cost Cyclone V FPGA (5CEBA7 series, Intel) that implements all core functions, including discharge control and data buffering. An external 128-Mb EPCS flash memory stores the FPGA firmware via active serial (AS) configuration. For debugging, a low-jitter 200-MHz oscillator (DSC1103, Microchip) on the FPGA board drives a phase-locked loop in the FPGA, providing global clocks for firmware development. A USB-to-UART bridge chip (CP2103, Silicon Labs) operating at 921600 bps transmits detector

data and debug information, with a B-type USB connector enabling plug-and-play communication with a PC. A mini display port supports external clock distribution, synchronization, and communication. Four LVDS I/O port pairs with a maximum rate of 1.25 Gbps enable user-defined command communications and detector data transmissions, allowing multiple FEE modules to be conveniently scaled into large-scale distributed particle detector systems.

Most low voltages on the FPGA board, such as 1.8 V and 2.5 V, are generated by low-dropout (LDO) linear regulators (TPS74401, TI). However, the V_{Thr} voltage is supplied by a separate LDO regulator (LT3080, Analog Devices) supporting adjustable output down to zero. In experiments, V_{Thr} thresholds for positive and negative charge signals were set to 2.47 V and 30 mV, respectively. Two SS4 connectors facilitate board-to-board interconnection with the analog board. Notably, the voltage comparators and 3-state buffers in the linear discharge scheme are implemented using digital LVDS receivers and digital low-voltage complementary metal oxide semiconductor output ports in the FPGA, respectively. Fig. 4 [Figure 4: see original paper] shows the customized FPGA board, which shares the same 70 × 70 mm^2 dimensions as the analog board. The two boards connect via board-to-board connectors (SS4 and ST4 series).

3.3 FPGA firmware

The firmware framework of the FEE system is depicted in Fig. 5 [Figure 5: see original paper]. The internal functional blocks include: (1) an LVDS comparator and 3-state buffer array for 64-channel linear discharge implementation, (2) charge calculation and timing pickoff using FPGA counters, (3) event buffering and formatting, and (4) communication interfaces comprising the UART engine and LVDS data engine. In the final design, the UART engine serves debugging purposes, while the LVDS interface supports system integration. Additionally, time measurement involves high-precision TDC implementation based on the FPGA carry chain [**?**], which is currently under development. For performance evaluations of the FEE in SiPM detector applications, only a coarse counter was employed.

4 Evaluation experiments

Evaluation experiments for the FEE are divided into two categories: electronics tests and detector tests. All experiments were conducted at room temperature, with the experimental setup described below.

4.1 Electronics test setup

The electronics evaluation experiments measured noise, channel linearity, and uniformity. Baseline fluctuations of the op amp were used to quantify analog board noise, which was observed using an oscilloscope and histogrammed to determine the root mean square (RMS) noise value. Channel linearity, critical

for particle detector FEE, was assessed using a pulse generator (AFG3252, Tektronix) driving a capacitor C_G = 200 pF. The relationship between charge and QDC digital codes was obtained by incrementing the pulse amplitude V_G, corresponding to an injected charge Q = C_G × V_G. The pulse generator was controlled to provide 50 mV amplitude steps (10 pC/step), with QDC pulse widths measured using a coarse counter. Sixty-four-channel data were packaged and transmitted to a host PC for post-processing, acquiring 2000 events at each amplitude step to determine mean values. In electronics tests, the standard deviation in histograms was negligible. The calculated mean values were plotted and fitted using least-squares estimation, with the experimental setup block diagram shown in Fig. 6 [Figure 6: see original paper].

Channel uniformity was evaluated using the distributions of fitted slopes and intercepts, with slope uniformity expressed as mean ± standard deviation. Notably, half of the QDC channels were configured for negative polarity inputs, while the other half were configured for positive polarity during linearity testing.

4.2 Detector setup

An 8 × 8 SiPM array (S13361-3050, Hamamatsu) was used to evaluate the dual-polarity multi-channel FEE. The SiPM array measures 25.8 mm, with each pixel covering a 3 × 3 mm^2 active area and a 0.2 mm gap between adjacent pixels. The breakdown voltage V_{BR} is 53 V, with an operating voltage of V_{BR} + 2.4 V applied in our experiments via a DC power supply (E3617A, Agilent). A 15 × 15 LYSO crystal array (Epic Crystal Co., Ltd.) generates light signals, with each crystal bar measuring 1.535 × 1.535 × 20 mm^3. Four lateral surfaces of each LYSO crystal bar are unpolished, while the two ends are polished. Enhanced specular reflectors with 0.065 mm thickness are placed between crystals, resulting in a 1.6 mm center-to-center distance between adjacent crystals. The scintillator-SiPM combination forms a PET detector, with the LYSO array directly coupled to the SiPM using silicon grease. A half-crystal shift achieves 4-to-1 coupling, positioning the LYSO array at the center of the SiPM [**?**]. The PET detector was irradiated using a Na-22 point source, with the FPGA programmed to automatically perform event triggering, charge and timing calculations, data formatting, and UART communication with a host PC.

The SiPM array was configured using three readout methods. In the first configuration, all cathodes are connected, and charges are read out through 64-channel anode electrodes, inducing positive charge signals and configuring all 64 FEE channels for positive polarity (V_{stage} at op amp noninverting ports). In the second scheme, all anodes are connected, with signals from cathode electrodes fed to the 64-channel FEE, producing negative polarity signals and configuring the analog board for negative-polarity input mode (V_{offset} at all op amp noninverting ports). Both schemes employ 64-channel signals for energy-weighted positioning. When a particle strikes a crystal bar, thousands of visible photons are generated and transmitted along the bar, dividing into several por-

tions upon reaching the SiPM pixel sensitive surface—this is known as the "light-sharing mechanism" [?]. Depending on the bar location, light divides into 1, 2, or 4 parts received by adjacent SiPM pixels. The fired crystal bar coordinates (X, Y) based on energy-weighted positioning are expressed as:

$$X = \frac{\sum_i \sum_j Q_{ij} x_j}{\sum_i \sum_j Q_{ij}}$$

$$Y = \frac{\sum_i \sum_j Q_{ij} y_i}{\sum_i \sum_j Q_{ij}}$$

where x_j and y_i are the relative coordinates of SiPM pixels along columns and rows, respectively, i and j are row and column indices, and Q_{ij} is the total charge at each pixel output.

The third readout scheme, presented in our previous study [?], combines anodes and cathodes into 8-row and 8-column outputs, respectively, referred to as "8+8 SiPM." Specifically, anodes in each row are connected, while cathodes in each column are connected. This configuration requires only eight positive-polarity and eight negative-polarity electronics channels, using a single FH12 series connector on the analog board to connect to the adapter board. The energy-weighted position (X, Y) simplifies to:

$$X = \frac{\sum_i Q_{ci} x_i}{\sum_i Q_{ci}}$$

$$Y = \frac{\sum_i Q_{ri} y_i}{\sum_i Q_{ri}}$$

where Q_{ci} and Q_{ri} are the readout charges along columns and rows, respectively, and x_i and y_i are the relative SiPM pixel coordinates. Leveraging the dual-polarity QDC scheme, the 8+8 SiPM configuration reduces the number of readout electronics channels, facilitating large-scale, multi-channel detector development. Fig. 7 [Figure 7: see original paper] shows three adapter boards with different configurations.

In the first two configurations, one end of the LYSO array is coupled to a SiPM, while the other end is sealed with Teflon tape. Crystal position decoding maps, also called "crystal discrimination maps," were generated using an energy-weighted algorithm and evaluated qualitatively via profile analysis. In the third configuration, the LYSO crystal array was coupled with two 8+8 SiPMs at both ends, utilizing 32 electronics channels for dual-end readout. This configuration provides dual-end energy information, enabling energy spectrum plotting with resolution determined by full width at half maximum. Fig. 7 shows the detectors and adapter boards for all three readout configurations.

5.1 Electrical Performance

Fig. 8 [Figure 8: see original paper] shows the baseline and noise spectrum from one negative-polarity channel, revealing a baseline offset of -1.233 mV originating from op amp input bias current and unbalanced parameters at differential input ports. Gaussian fitting yields an RMS noise of 1.357 mVrms. Baselines for all channels were measured to establish a unified threshold V_{Thr} across all electronics channels. Fig. 9 [Figure 9: see original paper] presents error bar plots illustrating baseline offset and noise distribution across all 64 channels, with all channels configured in negative-polarity input mode for noise measurement. Electronics noise arises from resistor thermal noise and op amp intrinsic noise, with resistor values (R_{discharge} and R_L) below 50 kΩ recommended for optimal electrical performance.

Fig. 10 [Figure 10: see original paper] shows typical signal waveforms and discharge waveforms from linearity tests for negative and positive charge injections. Linearity test results for dual-polarity charge channels are presented in Fig. 11 [Figure 11: see original paper]. The correlation coefficient R from linear least-squares estimation quantifies the degree of linear correlation, with R^2 referred to as the linearity of the estimate. To compare positive and negative channels, half of the 64 channels were configured for negative-polarity input and half for positive polarity. As shown in Fig. 11, linearity results differ slightly between positive and negative channels, with intercept differences arising from nonuniform baselines under different configurations—easily correctable when necessary. Both channel types exhibit excellent linearity with correlation coefficients R^2 = 0.998. Equation (2) indicates that fewer factors affect linearity compared to traditional readout electronics comprising preamplifiers, main amplifiers, and ADCs [**?**]. Fig. 12 [Figure 12: see original paper] shows slope distributions for 32 positive-polarity and 32 negative-polarity channels, with means and standard deviations of 0.786 ± 0.009 and 0.795 ± 0.008, respectively. These linearity results demonstrate excellent uniformity across all 64 channels, enabling detector experiments without electronics calibration or correction.

5.2 Detector Results

Fig. 13 [Figure 13: see original paper] shows typical crystal discrimination maps for a 15 × 15 array of 1.5 × 1.5 × 20 mm^3 LYSO crystals irradiated by a Na-22 point source, with all crystals clearly distinguished. The left map corresponds to the first detector configuration reading out 64-channel anode signals for positioning, while the middle map shows the second configuration. Profile analysis of selected rows indicates peak-to-valley ratios (PVRs) of 12.1 and 14.4 for the first and second configurations, respectively, demonstrating the FEE system' s excellent readout capability for dual-polarity current signals. Fig. 13(c) shows a one-end crystal map for a 15 × 15 LYSO array coupled with two 8+8 SiPMs at both ends, with one-row profile analysis revealing an average PVR of 13.5 under the 8+8 SiPM readout configuration.

Dual-end readout of the LYSO array produces good energy spectra for PET development, with energy resolutions for 511-keV gamma photons across all crystals ranging from 14.4% to 18.2%. Resolution degrades at map edges due to light leakage. Fig. 14 [Figure 14: see original paper] shows a typical energy spectrum for a selected crystal, with 16.8% energy resolution at 511 keV. Notably, only negative-charge signals were used for dual-end energy summation.

Overall, the dual-polarity QDC demonstrates good performance in noise, linearity, and uniformity. In electronics tests, trigger thresholds of 30 mV and 2.47 V were selected for negative and positive charge measurements, respectively, with a 30 mV difference between trigger threshold and op amp output baseline for both polarities. Based on measured electronics noise, this threshold could be reduced to 10 mV to improve timing pickoff when fine-time measurement is enabled.

In the Cyclone V FPGA, the pulse width after the LVDS comparator is digitized by a coarse counter driven by a 200-MHz system clock. With a discharge resistor R_{discharge} of 10 kΩ, Eq. (2) yields:

$$\mathrm{LSB} = \frac{25.1\ \mathrm{pC}}{V_{IO} \cdot F_S \cdot R_{discharge}} = 1.25\ \mathrm{pC}$$

The discharge resistor R_{discharge} can be increased to improve measurement accuracy, but this widens the discharge time. During discharge, the QDC circuit cannot accept another signal [**?**], requiring a tradeoff between accuracy and count rate.

In detector experiments, three PET detector readout configurations verified the dual-polarity QDC circuit capability. The first two configurations employed single-end readout for the LYSO array. Upon gamma event detection in an LYSO crystal bar, generated light signals transmit along the bar. In single-ended readout, one portion of light is detected by corresponding SiPM pixels, while the remainder transmits along the bar and reflects off Teflon tape before being received by SiPM pixels. Compared to dual-end readout in the third configuration, more light escapes from the crystal bar, degrading energy resolution. Calculated energy resolutions for the first two configurations range from 24% to 30%. Fig. 15 [Figure 15: see original paper] shows typical energy spectra for selected crystals in these configurations, obtained by summing 64-channel positive signals in the first configuration and 64-channel negative signals in the second. Notably, the 511-keV photon peak value for positive charge is lower than for negative charge because holes have shorter drift lengths, and severe hole trapping in the semiconductor detector reduces the induced signal on the electrode [**?**].

6 Conclusion

With continuous SiPM technology advancement, FEE systems for SiPM signal processing are highly sought after across many research fields. Leveraging the FPGA-based QDC scheme, we designed and developed a compact 64-channel FEE system for SiPM-based radiation detectors. The FEE can process dual-polarity charge signals from detectors and demonstrates good electronics performance in noise, linearity, and uniformity. A PET detector with different readout configurations evaluated the FEE, showing good crystal discrimination maps under all three configurations and good energy resolution under dual-end readout. Overall, the FPGA-QDC-based FEE shows promising potential for applications in SiPM-based radiation detectors.

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Note: Figure translations are in progress. See original paper for figures.