Carrier Recovery and Timing Synchronization of GMSK Signals for Space Communications (Post-print)

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Date: 2019-04-01T00:00:00+00:00

Abstract

In space communications, excessive Doppler shift and Doppler rate hinder carrier recovery and clock synchronization in coherent demodulation receivers. To address this issue, a reliable and expedient improved squaring loop method is proposed for Gaussian Minimum Shift Keying (GMSK) signals to overcome large Doppler shifts. Initially, a coarse carrier frequency is acquired through a frequency estimation module, followed by the application of an improved squaring loop structure to realize carrier recovery and clock synchronization for GMSK signals. Simulation results demonstrate that under the conditions of input signal-to-noise ratio Eb/N0=5 dB and loop noise bandwidth of 50 kHz, the locking time for both the carrier recovery loop and clock synchronization loop is approximately 3.6 ms. Under low signal-to-noise ratio and large Doppler shift conditions, the proposed method can rapidly and stably achieve carrier recovery and clock synchronization for GMSK signals in space communications.

Full Text

Preamble

Vol. 37 No. 5
Application Research of Computers
ChinaXiv Partner Journal

Carrier Recovery and Clock Synchronization of GMSK Signals in Space Communications

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Abstract: In space communications, excessive Doppler shift and Doppler rate prevent coherent demodulation receivers from performing carrier recovery and clock synchronization. To address this, we propose a reliable and fast improved square-loop method for Gaussian Minimum Shift Keying (GMSK) signals to overcome large Doppler shifts. First, a coarse carrier frequency is obtained through a frequency estimation module, followed by carrier recovery and clock synchronization of the GMSK signal using an improved square-loop structure. Simulation results show that under input SNR of $E_b/N_0 = 5$ dB and loop noise bandwidth of 50 kHz, the carrier recovery loop and clock synchronization loop achieve lock in approximately 3.6 ms. Under conditions of low SNR and large Doppler shifts, this method can rapidly and stably implement carrier recovery and clock synchronization for GMSK signals in space communications.

Keywords: space communications; GMSK; Doppler shift; Doppler rate; square-loop

0 Introduction

Due to the scarcity of X-band spectrum allocation in deep-space communication missions, deep-space missions have begun to shift to Ka-band for data communications. However, X-band communication systems remain necessary for emergency communications [1,2]. To address challenges such as limited spectrum resources, high data rates, and long transmission distances, the Gaussian Minimum Shift Keying (GMSK) modulation scheme has been recommended by the Consultative Committee for Space Data Systems (CCSDS) as one of the deep-space communication modulation methods due to its constant envelope and high spectral efficiency [3~5]. In 2008, the European Space Agency (ESA) first applied GMSK modulation to the Herschel-Planck satellite test mission [6].

GMSK signal demodulation includes both non-coherent and coherent approaches. Traditional GMSK demodulation typically uses non-coherent methods, which offer simpler receiver design but suffer from performance degradation compared to coherent demodulation. In specialized fields such as space communications, non-coherent demodulation has a demodulation threshold limitation, making coherent demodulation the only viable approach for receiving GMSK signals.

In GMSK coherent demodulation receivers, phase-locked loop (PLL) structures are typically employed for coherent carrier extraction, with square-loop and Costas loop being the two most widely used loops in carrier recovery. In loop design, loop capture bandwidth and locking precision are contradictory requirements. Particularly in space communications, received signals often exhibit large Doppler shifts and Doppler rates. For example, in Mars exploration missions, the maximum Doppler shift can reach approximately 90 kHz, with a maximum Doppler rate of 1000 Hz/s [7]. Increasing the capture range requires increasing the loop noise bandwidth, which under low SNR conditions leads to degraded

locking precision. Therefore, practical applications require a compromise to meet engineering performance requirements. Meanwhile, automatic frequency control (AFC) loops can also complete carrier recovery and frequency offset estimation for certain modulated signals [8,9], typically applied in burst communications with fast carrier recovery, though their locking precision often fails to meet requirements under low SNR conditions.

In engineering applications for carrier recovery and frequency offset estimation, literature [10,11] proposes using universal digital loops for GMSK signal carrier recovery. However, due to the sinusoidal phase detection characteristics, the phase detection curve does not exhibit linear behavior under large error signals. Literature [12] proposes an FPGA-based linear all-digital phase-locked loop using the CORDIC (Coordinate Rotation Digital Computer) algorithm to extend the linear phase detection range. For large Doppler shifts encountered in space communications, literature [13] proposes a fast and accurate carrier recovery method based on FFT algorithms with simple structure and high estimation precision, which accelerates PLL locking through frequency estimation. Literature [14,15] presents maximum likelihood frequency offset estimation methods for QPSK signals with complex FPGA design but high estimation accuracy. Literature [16] proposes optimized algorithms on FFT frequency offset estimation to improve precision, though practical engineering implementation is difficult.

To achieve carrier recovery and clock synchronization for GMSK signals under large Doppler shifts and low SNR conditions, this paper combines previous work and proposes an improved square-loop method that integrates square-loop with automatic frequency control loop. The FPGA implementation based on the CORDIC algorithm completes linear phase detection for the square-loop. To achieve simple yet accurate frequency offset estimation, an automatic control loop design based on FFT algorithms is employed to assist the square-loop in carrier recovery. This paper presents a feasible approach for FPGA implementation of GMSK signal carrier recovery and clock synchronization in space communications.

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1 Problem Analysis

Space vehicles, including artificial satellites, manned spacecraft, and space shuttles, operate at high velocities in orbit. Consequently, the signals received on the ground inevitably exhibit Doppler phenomena, which include Doppler shift and Doppler rate [17]. The magnitude of these values is crucial for PLL parameter design.

As shown in [Figure 1: see original paper], using a low Earth orbit as a template, we assume a space vehicle undergoes approximately circular motion around Earth with the ground receiver in the same plane as the vehicle' s orbit. We analyze the Doppler phenomenon in communication between the ground receiver and space vehicle based on the vehicle' s trajectory diagram.

[**Figure 1: see original paper**] *Aircraft motion trajectory plan*

Establishing a coordinate system with Earth' s center O as the origin, where R represents the ground receiver position, S represents the current space vehicle position, r_e is Earth' s radius, h is orbital altitude, v_s is the linear velocity at point S, and assuming the vehicle moves from point B to S with rotation angle θ, α is the angle between $\overrightarrow{RS}$ and $\overrightarrow{OS}$. From Newton' s law of universal gravitation:

$$\begin{cases} v_s = \sqrt{\frac{GM}{r}} \\ \omega = \sqrt{\frac{GM}{r^3}} \\ r = r_e + h \end{cases}$$

where r is the vehicle' s orbital radius, ω is the vehicle' s angular velocity, G is the gravitational constant, and M is the mass of the central body (Earth' s mass in this case).

According to the Doppler shift calculation formula, the Doppler shift f_d is:

$$f_d = \frac{v_{sr}}{c} f_t$$

where v_{sr} is the velocity component of the vehicle' s linear velocity v_s along the vector $\overrightarrow{RS}$, f_t is the radio signal transmission frequency, and c is the speed of light.

From velocity decomposition:

$$v_{sr} = v_s \sin\alpha$$

$$\sin\alpha = \frac{r_e \sin\theta}{\sqrt{r_e^2 + r^2 - 2r_e r\cos\theta}}$$

Substituting equations (3) and (4) into equation (2) yields:

$$f_d = \frac{v_s f_t}{c} \cdot \frac{r_e \sin\theta}{\sqrt{r_e^2 + r^2 - 2r_e r\cos\theta}}$$

The Doppler rate $\dot{f}_d$ is the change in Doppler shift per unit time t, obtained by differentiating f_d with respect to time t:

$$\dot{f}_d = \frac{df_d}{dt}$$

As shown in Figure 1, normal signal transmission and reception can only occur when the vehicle is within the arc $\widehat{BA}$ range, i.e., $0^\circ \leq \theta \leq 180^\circ$.

Based on the above derivations, for X-band radio signal transmission frequency $f_t = 8.4$ GHz, we analyze the Doppler phenomenon characteristics by varying the vehicle' s altitude.

[Figure 2: see original paper] *Doppler shifts of receive signals*

As shown in [Figure 2: see original paper], lower vehicle altitude results in larger maximum Doppler shift. At an altitude of 500 km, the maximum Doppler shift can reach approximately 200 kHz, with the minimum Doppler shift of 0 Hz occurring at $\theta = 90^\circ$.

[Figure 3: see original paper] *Doppler rate of receive signals*

As shown in [Figure 3: see original paper], lower vehicle altitude also results in larger maximum Doppler rate. At 500 km altitude, the maximum Doppler rate can reach approximately 3 kHz, with the maximum Doppler rate occurring at $\theta = 90^\circ$.

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2 GMSK Carrier Recovery and Clock Synchronization Method

GMSK signals are generated by passing symbol signals through a narrowband Gaussian filter before MSK modulation, which can also be interpreted as continuous-phase frequency shift keying (CPFSK) with a modulation index of 0.5 [18]. Since wireless communication employs suppressed-carrier modulation, although the received signal itself contains no carrier frequency component, it does contain carrier frequency information that can generate carrier frequency multiplication components through nonlinear transformation.

2.1 GMSK Signal Analysis

Based on MSK modulation characteristics, the phase change per symbol period is $\pm\pi/2$ (T_b is the symbol period). Therefore, the frequency variation range per symbol period in GMSK signals is:

$$f_c \pm \frac{1}{4T_b}$$

where f_c is the carrier frequency.

Assuming the input signal is:

$$x(t) = s(t) + n(t)$$

where:

$$s(t) = \sqrt{2}\sin\left[2\pi f_c t \pm \frac{\pi}{2T_b} m(t)t\right]$$

$n(t) = n_c(t) + jn_s(t)$ is independent additive white Gaussian noise, and ω_c is the carrier angular frequency.

After squaring and bandpass filtering, the GMSK signal becomes:

$$y(t) = [s(t) + n(t)]^2 = s^2(t) + 2s(t)n(t) + n^2(t)$$

From equation (10), the squared signal contains discrete frequencies $2f_H$ and $2f_L$. The squared spectrum of the GMSK signal is shown in [Figure 4: see original paper].

[Figure 4: see original paper] *Spectrum of GMSK signal square*

The relationship between carrier frequency and discrete frequencies is:

$$\begin{cases} f_H = f_c + \frac{1}{4T_b} \\ f_L = f_c - \frac{1}{4T_b} \end{cases}$$

By obtaining the $2f_H$ and $2f_L$ discrete frequency signals and mixing them followed by low-pass filtering, we can obtain a clock frequency signal of $f_b = \frac{1}{2T_b}$, which after pulse shaping can extract the clock.

2.2 Improved Square Loop Analysis and Design

The digital square loop is a type of digital phase-locked loop comprising a phase detector, loop filter, and Numerically Controlled Oscillator (NCO). Square loop design requires analysis of both digital and analog PLLs to determine loop parameters. Literature [19] provides detailed analysis of digital PLL design based on second-order analog PLLs. The improved square-loop structure proposed in this paper is shown in [Figure 5: see original paper].

[Figure 5: see original paper] *Modified square loop structure diagram*

2.2.1 All-Digital PLL Model Analysis The S-domain transfer function of the loop filter is:

$$F(s) = \frac{1 + s\tau_2}{s\tau_1}$$

[Figure 6: see original paper] *Second-order analog phase-locked loop phase model*

[Figure 6: see original paper] shows the phase model of a second-order analog PLL, where K_d is the phase detector gain, and the VCO S-domain transfer function is:

$$V(s) = \frac{K_o}{s}$$

The phase detector output error voltage is:

$$V_d(s) = K_d[\theta_1(s) - \theta_2(s)]$$

After loop filter filtering, the control voltage is:

$$V_c(s) = F(s)V_d(s)$$

The analog PLL phase model' s S-domain transformation formula in the linear phase detection region is:

$$\theta_2(s) = \frac{K_o V_c(s)}{s}$$

The S-domain transfer function of the analog PLL is:

$$H(s) = \frac{K_d K_o F(s)}{s + K_d K_o F(s)} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

where K_o is the VCO gain, τ_1 and τ_2 are time constants, ω_n is the loop natural angular frequency, and ξ is the damping factor.

To digitize the analog PLL, we use the bilinear transformation method [20]. The transformation formula is:

$$s = \frac{2}{T_s} \cdot \frac{z-1}{z+1}$$

where T_s is the digital sampling period.

Substituting equation (15) into equations (12) and (13) yields:

$$F(z) = \frac{C_1 + C_2 z^{-1}}{1 - z^{-1}}$$

$$N(z) = \frac{K_o T_s}{2} \cdot \frac{z+1}{z-1}$$

where:

$$\begin{cases} C_1 = \frac{\tau_2}{T_s} + \frac{\tau_1}{2T_s} \\ C_2 = \frac{\tau_2}{T_s} - \frac{\tau_1}{2T_s} \end{cases}$$

[Figure 7: see original paper] *Second-order digital phase-locked loop phase model*

The digital PLL phase model is shown in [Figure 7: see original paper]. The z-domain transfer function can be expressed as:

$$H(z) = \frac{\theta_2(z)}{\theta_1(z)} = \frac{K_d F(z) N(z)}{1 + K_d F(z) N(z)}$$

where $K = K_d K_o$ is the total digital loop gain.

The smaller the loop noise bandwidth, the smaller the phase variance σ^2 and the smaller the steady-state fluctuation. For an ideal second-order loop filter, the loop noise bandwidth B_L can be expressed as:

$$B_L = \frac{\omega_n}{8\xi}\left(1 + 4\xi^2\right)$$

The loop signal-to-noise ratio $(S/N)_L$ is defined as the ratio of input signal power to single-sideband noise power, representing the loop' s noise suppression capability. Typically, the loop can only lock normally when $(S/N)_L \geq 6$ dB, expressed as:

$$\left(\frac{S}{N}\right)_L = \frac{S_i}{N_i} \cdot \frac{B_i}{2B_L}$$

where S_i/N_i is the input SNR, B_i is the input signal bandwidth, and B_L is the loop noise bandwidth.

From the above analysis, we can derive:

$$\omega_n \leq \frac{3}{4} \cdot \frac{S_i}{N_i} \cdot \frac{B_i}{\xi}$$

For frequency ramp signals with frequency change rate R, the second-order PLL maintains loop stability when:

$$R \leq \frac{\omega_n^2}{2}$$

Combining equations (22), (23), and (27) determines the range of the loop natural angular frequency ω_n:

$$\begin{cases} \omega_n \leq \sqrt{\frac{3}{4} \cdot \frac{S_i}{N_i} \cdot \frac{B_i}{\xi}} \\ \omega_n \geq \sqrt{2R} \end{cases}$$

2.2.2 Improved Square Loop Parameter Calculation Assuming the phase detector input signal is:

$$u_i(t) = U_i \cos(\omega_1 t + \theta_1(t))$$

where ω_1 is the input signal angular frequency and $\theta_1(t)$ is the input signal initial phase.

The NCO output local oscillator signal can be expressed as:

$$\begin{cases} u_o^I(t) = U_o \cos(\omega_2 t + \theta_2(t)) \\ u_o^Q(t) = U_o \sin(\omega_2 t + \theta_2(t)) \end{cases}$$

where ω_2 is the local oscillator angular frequency and $\theta_2(t)$ is the local oscillator initial phase.

After mixing the input signal with the local oscillator signal and low-pass filtering to remove high-frequency components, we obtain:

$$\begin{cases} u_{Ie}(t) = \frac{U_i U_o}{2} \cos[\theta_1(t) - \theta_2(t)] \\ u_{Qe}(t) = \frac{U_i U_o}{2} \sin[\theta_1(t) - \theta_2(t)] \end{cases}$$

The arctangent phase detector output error signal is:

$$u_d(t) = \arctan\left(\frac{u_{Qe}(t)}{u_{Ie}(t)}\right) = \theta_e(t)$$

where $\theta_e(t) = \theta_1(t) - \theta_2(t)$ is the phase error.

Thus, the arctangent phase detector gain is:

$$K_d = 1$$

The phase variance σ^2 under input signal with additive white Gaussian noise can be expressed as:

$$\sigma^2 = \frac{B_L}{(S/N)_L}$$

[**Figure 8: see original paper**] *Arctangent Phase discrimination schematic*

[**Figure 9: see original paper**] *Numerically controlled oscillator schematic*

The Numerically Controlled Oscillator (NCO) generates orthogonal sine and cosine samples. According to PLL operation principles, the control voltage from the loop filter corrects the NCO output frequency:

$$f_{out} = f_0 + \frac{W}{2^N} f_s$$

where f_s is the sampling frequency, N is the phase accumulator word length, W_0 is the initial frequency word, and ΔW is the control frequency word.

The NCO phase gain is:

$$K_o = \frac{2\pi f_s}{2^N}$$

where T_{dds} is the phase accumulator update period. In engineering applications, $T_{dds} = T_s$.

Through factor removal, the pseudo-rotation formula can be obtained as:

$$\begin{cases} x_{i+1} = x_i - d_i \cdot 2^{-i} y_i \\ y_{i+1} = y_i + d_i \cdot 2^{-i} x_i \\ z_{i+1} = z_i - d_i \cdot \arctan(2^{-i}) \end{cases}$$

where $d_i = \mathrm{sgn}(z_i)$ determines the rotation direction at each iteration.

In the improved square-loop structure shown in [Figure 5: see original paper], input signal bit-width changes introduce additional gain. The loop filter gain K_l can be re-expressed as:

$$K_l = \frac{2^{B_d}}{2^{B_o}} \cdot K_d K_o$$

where B_d is the loop filter output bit-width and B_o is the NCO output bit-width.

In space communications, signal processing involves down-converting high-frequency signals to intermediate frequency for data processing. In this paper, the digital signal sampling rate $f_s = 50$ MHz, carrier frequency $f_c = 10$ MHz, information rate $f_b = 1$ MHz, resulting in GMSK input signal bandwidth $B_i = 500$ kHz.

Based on the Doppler phenomenon analysis in [Figure 2: see original paper] and [Figure 3: see original paper], the maximum Doppler shift is 200 kHz and the maximum Doppler rate is 3 kHz. According to carrier estimation frequency offset accuracy, the fast capture range $\Delta\omega_L$ is at most 3 kHz, frequency change rate R is at most 3 kHz, and input SNR $E_b/N_0 = 5$ dB. With damping factor $\xi = 0.707$, phase detector gain $K_d = 1$, frequency word bit-width $N = 32$ to improve PLL precision, and loop filter bit-width $B_d = 29$, we can set ω_n as:

$$\omega_n = 3.25 \times 10^5 \text{ rad/s}$$

based on equations (28) and (35), balancing lock time and steady-state phase error.

From equations (35), (26), and (18)(20), we can calculate the improved square-loop z-domain transfer function:

$$H(z) = \frac{0.0267z^{-1} + 0.0263z^{-2}}{1 - 1.9733z^{-1} + 0.9737z^{-2}}$$

From equation (37), the improved square-loop poles are:

$$z = 0.9867 \pm 0.0132i$$

Since the poles are located inside the unit circle, this proves the loop is stable.

2.3 CORDIC Phase Detection FPGA Implementation

The CORDIC algorithm can convert trigonometric function calculations into addition, subtraction, and shift operations, making it highly suitable for hardware circuit implementation. This algorithm not only saves FPGA hardware resources but also significantly improves calculation speed [22]. The CORDIC algorithm coordinate rotation diagram is shown in [Figure 10: see original paper].

[Figure 10: see original paper] *Coordinate rotation diagram*

where z is the accumulated iteration angle, each iteration rotation angle is $\arctan(2^{-i})$, whose values can be obtained through look-up tables as shown in . $d_i = \text{sgn}(z_i)$ determines the rotation direction at each step.

**** *Rotation angle value*

The CORDIC phase discrimination curve is shown in [Figure 11: see original paper].

[Figure 11: see original paper] *CORDIC algorithm phase discrimination curve*

2.4 Carrier Frequency Estimation FPGA Implementation

The PLL capture time is directly related to the initial frequency difference—the larger the initial frequency difference, the longer the capture time. Limited by PLL performance requirements with small capture bandwidth, large frequency offsets prevent local carrier and phase synchronization, making coherent demodulation impossible. By analyzing the input signal to determine the coarse carrier frequency, the initial frequency difference can be controlled within a small range, facilitating fast PLL capture.

The frequency estimation module block diagram is shown in [Figure 12: see original paper].

[**Figure 12: see original paper**] *Frequency estimation schematic*

The core of the frequency estimation module is the N-point FFT operation (using IP core). After performing FFT on N input signal points, the magnitude is calculated and the position of the maximum amplitude (spectral line point) is found. The estimated value is determined through the spectral line point position and finally converted to a frequency word output.

This method is based on FFT algorithm for frequency estimation with simple structure. Simulation of estimation precision for GMSK signals with input SNR of 5 dB and frequency shift in the range of -300 kHz to 300 kHz is shown in [Figure 13: see original paper], demonstrating that it meets Doppler shift estimation requirements.

[**Figure 13: see original paper**] *FFT carrier estimation simulation diagram*

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3 Experiments and Discussion

This paper uses Altera' s Cyclone IV series EP4CE75F23C8 chip, with joint simulation testing using QuartusII, ModelSim, and MATLAB to evaluate the performance of traditional square-loop versus improved square-loop under large Doppler shifts and different SNR conditions.

Test input conditions: GMSK modulation, sampling rate of 50 MHz, carrier frequency of 10 MHz, initial frequency offset of 250 kHz, Doppler rate of 3 kHz/s, information rate of 1 Mbps.

3.1 Traditional Square Loop Structure

The traditional square loop contains only three main modules: phase detector, loop filter, and Numerically Controlled Oscillator (NCO), where the phase detector typically uses a sinusoidal phase detector for approximate linear phase detection.

Experiment 1: Traditional square loop structure for GMSK modulated signal carrier recovery and clock synchronization with input SNR of 20 dB. ModelSim simulation is shown in [Figure 14: see original paper].

[Figure 14: see original paper] *Carrier recovery and clock synchronization ($E_b/N_0 = 20$ dB)*

In [Figure 14: see original paper], the loop filter outputs of both carrier recovery loop ($frequency\_df\_c$) and clock synchronization loop ($frequency\_df\_s$) converge, indicating that under input SNR of 20 dB and small frequency difference, the traditional square loop can complete GMSK signal carrier recovery and clock synchronization. The carrier frequency estimation module obtains the frequency word in approximately 1.2 ms, controlling the frequency difference to about 2197 Hz. The traditional square loop with natural angular frequency of 50 kHz completes carrier and clock loop locking in about 5.5 ms.

Experiment 2: With input SNR of 5 dB, ModelSim simulation is shown in [Figure 15: see original paper] and [Figure 16: see original paper].

[Figure 15: see original paper] *Carrier recovery and clock synchronization ($E_b/N_0 = 20$ dB)*
[Figure 16: see original paper] *Carrier recovery and clock synchronization ($E_b/N_0 = 5$ dB)*

In [Figure 16: see original paper], under SNR of 5 dB, the loop filter outputs of both carrier recovery loop ($frequency\_df\_c$) and clock synchronization loop ($frequency\_df\_s$) fail to converge. The loop cannot achieve carrier recovery and clock synchronization, demonstrating that the traditional square loop cannot maintain stability under low SNR conditions.

3.2 Improved Square Loop Structure

The improved square-loop structure proposed in this paper adds a carrier estimation module to the square loop to counter large Doppler shifts, reducing initial frequency difference while using FPGA implementation of the CORDIC algorithm for linear phase detection to reduce phase detection error and improve PLL stability.

Experiment 3: Improved square-loop structure with input SNR of 20 dB. ModelSim simulation is shown in [Figure 17: see original paper].

[Figure 17: see original paper] *Carrier recovery and clock synchronization ($E_b/N_0 = 20$ dB)*

The data in [Figure 17: see original paper] including loop filter output, carrier output *dout*, and clock signal *b_clk* were analyzed using MATLAB, with results shown in [Figure 18: see original paper] and [Figure 19: see original paper].

[Figure 18: see original paper] *Carrier loop simulation data map ($E_b/N_0 = 20$ dB)*

[Figure 19: see original paper] *Carrier output simulation data map ($E_b/N_0 = 20$ dB)*

After approximately 1.2 ms of frequency offset estimation, the initial frequency offset is controlled to about 2197 Hz. The improved square loop with natural angular frequency of 50 kHz achieves phase lock in about 2 ms, outputting a coherent carrier at 10.25 MHz. [Figure 20: see original paper] shows the extracted clock signal period is 1 MHz. This demonstrates that under input SNR of 20 dB with large Doppler shift and fast Doppler rate, carrier recovery and clock synchronization are achieved in a short time.

[Figure 20: see original paper] *Clock synchronization loop simulation data diagram ($E_b/N_0 = 20$ dB)*

Experiment 4: Improved square-loop structure with input SNR of 5 dB. ModelSim simulation is shown in [Figure 21: see original paper].

[Figure 21: see original paper] *Carrier recovery and clock synchronization ($E_b/N_0 = 5$ dB)*

The data in [Figure 21: see original paper] including loop filter output, carrier output *dout*, and clock signal *b_clk* were analyzed using MATLAB, with results shown in [Figure 22: see original paper] and [Figure 23: see original paper].

[Figure 22: see original paper] *Carrier output simulation data map ($E_b/N_0 = 5$ dB)*
[Figure 23: see original paper] *Carrier output simulation data map ($E_b/N_0 = 5$ dB)*

The carrier frequency offset estimation similarly controls the frequency difference to about 2197 Hz. Compared with the 5 dB input SNR case, the frequency offset estimation time extends to approximately 2.2 ms, and loop lock time extends to about 3.6 ms, outputting a coherent carrier at 10.25 MHz. [Figure 24: see original paper] shows the clock signal output period is 1 MHz. This verifies that under input SNR of 5 dB with large Doppler shift and Doppler rate, the improved square loop can still stably achieve carrier recovery and clock synchronization.

[Figure 24: see original paper] *Clock synchronization loop simulation data diagram ($E_b/N_0 = 5$ dB)*

Comprehensive experiments demonstrate that the traditional square loop cannot guarantee stable operation under large Doppler shift, fast Doppler rate, and low SNR conditions. In contrast, the improved square-loop scheme proposed in this paper can complete GMSK signal carrier recovery and clock synchronization under large Doppler shift and low SNR conditions, while also improving loop lock speed and stability.

4 Conclusion

This paper provides a detailed analysis of the low SNR and Doppler phenomenon environment faced by GMSK signals in space communications, and proposes an FPGA-based improved square-loop method. Under low SNR conditions, this method rapidly overcomes Doppler effects to complete carrier recovery and clock synchronization in a short time. Joint simulation using QuartusII, ModelSim, and MATLAB demonstrates that the method overcomes the effects of large Doppler shift and fast Doppler rate. Under input SNR of 5 dB and loop noise bandwidth of 50 kHz, the carrier loop and clock synchronization loop achieve lock in approximately 3.6 ms. The stability under different noise environments meets engineering requirements, proving that the method satisfies the requirements for GMSK signal carrier recovery and clock synchronization in space communications.

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Note: Figure translations are in progress. See original paper for figures.