# A Controller Architecture for Modular Multilevel Converters Based on EtherCAT: Postprint

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## Abstract

Modular Multilevel Converters (MMCs) contain a large number of submodules, which significantly increases system complexity and cost of the control structure. Furthermore, traditional CAN or RS-485 communication exhibits low transmission rates and poor reliability, resulting in inadequate signal synchronization among submodules and difficulty in satisfying the requirements for coordinated operation and high-speed reliable communication among multiple controllers. To address this problem, this paper introduces EtherCAT industrial ethernet technology and proposes a controller architecture scheme for modular multilevel converters based on EtherCAT. Compared with conventional hierarchical control schemes, the proposed scheme consists of only two layers—master controller and slave controller—thereby simplifying the control structure while substantially improving the transmission rate and reliability between master and slave stations. Additionally, this scheme can precisely guarantee carrier signal synchronization among controllers. Based on this scheme, a three-phase MMC experimental platform was constructed, and experimental results validate the feasibility and correctness of the proposed approach.

## Full Text

## Preamble

### Controller Architecture of a Modular Multilevel Converter Based on EtherCAT

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## Abstract

Modular Multilevel Converters (MMCs) contain a large number of sub-modules, which significantly increases system complexity and cost. Traditional CAN or RS-485 communication suffers from slow transmission rates and low reliability, resulting in poor signal synchronization among sub-modules and failing to meet the requirements for coordinated operation and high-speed, reliable communication between multiple controllers. To address this issue, this paper introduces EtherCAT industrial Ethernet technology and proposes a controller architecture scheme for MMCs based on EtherCAT. Compared with traditional hierarchical control schemes, this proposed scheme simplifies the control structure by comprising only two layers—a master controller and slave controllers—while substantially improving transmission rate and reliability between master and slave stations. Moreover, the scheme can precisely ensure carrier signal synchronization among controllers. A three-phase MMC experimental platform was built based on this scheme, and experimental results demonstrate its feasibility and correctness.

**Keywords:** Modular Multilevel Converter (MMC), EtherCAT, carrier signal synchronization, real-time performance, experimental platform

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## 1 Introduction

Modular Multilevel Converters (MMC) [1] have become a research hotspot in recent years due to their advantages of easy scalability, simple redundancy control implementation, and low output harmonic content. Research has focused on their mathematical models [2-4], control methods [5-7], and hardware structures [8-10]. Currently, the primary field application is in High Voltage Direct Current (HVDC) transmission, while laboratory research mainly covers battery energy storage, photovoltaic power generation, motor drives, and power quality management.

The main circuit topology of the modular multilevel converter is shown in [Figure 1: see original paper]. The converter consists of six bridge arms, each comprising N sub-modules connected in series with a current-limiting arm inductor Larm. Each sub-module (SM) consists of a full-bridge module with four anti-parallel diodes. The DC side of the converter is paralleled with DC capacitors, while the AC side is drawn out and connected in series with inductor L.

In engineering applications, MMCs generally require dozens or even hundreds of cascaded sub-modules to achieve high voltage, large capacity, and high output waveform quality, which introduces several challenges. First, a single controller cannot handle the control tasks of an MMC, necessitating multi-controller coordinated control methods and reliable, high-speed, large-capacity communication to connect the controllers for data exchange, which increases the difficulty of multi-controller coordination. Second, high-potential isolation must be achieved between sub-modules and controllers while simultaneously ensuring precise synchronization of carrier signals among controllers, which significantly increases both the complexity and cost of the control system [11].

To address these issues, this paper designs a nine-level MMC experimental platform prototype based on EtherCAT and introduces real-time EtherCAT communication technology to propose an MMC system control scheme based on EtherCAT bus technology. This scheme includes only two layers—a PLC master controller and slave controllers—simplifying the control structure. Communication between the PLC master controller and each slave controller via EtherCAT data frames substantially improves transmission rate and reliability compared with traditional CAN communication modes [12]. Additionally, utilizing the clock synchronization function provided by EtherCAT technology can precisely ensure carrier signal synchronization among slave unit controllers, enhancing the scalability of the modular cascaded scheme. This is verified through experimental results.

## 2 Working Principle of Real-Time Ethernet EtherCAT

Ethernet for Control Automation Technology (EtherCAT) is an open-architecture fieldbus system based on Ethernet, proposed by German company Beckhoff Automation. Unlike traditional Ethernet solutions, EtherCAT employs a communication method similar to a "summation frame," which increases network data utilization and further improves real-time performance. EtherCAT networks adopt a master-slave structure, with only one master station in the network to monitor data transmission while remaining devices operate as slaves that exchange data according to the master station' s configuration.

The message processing at slave nodes in EtherCAT networks is completed directly by the EtherCAT Slave Controller (ESC) at the data link layer, reducing node data processing delay and thus improving data real-time performance. The network communication principle of EtherCAT is shown in [Figure 2: see original paper]. Furthermore, EtherCAT provides a precise distributed clock function for synchronizing the timing of various slaves.

### 3.1 Control Strategy of the MMC Experimental Prototype

The control strategy block diagram is shown in [Figure 3: see original paper]. The upper and lower arm energy sum controller regulates the total arm energy

by injecting a DC component idiff0. The energy difference controller regulates the energy difference between upper and lower arms by injecting a fundamental frequency component idiff1. The AC-side current controller is consistent with conventional two-level or multilevel current control and will not be elaborated here.

## 3.2 Control System Functional Description

The system control structure of the modular multilevel converter based on EtherCAT is shown in [Figure 4: see original paper]. The control system comprises three layers: monitoring station, master PLC, and slave controllers.

The monitoring station communicates with the master controller to implement control parameter distribution and command issuance while monitoring the overall system operation status. The monitoring station uses a PC with a human-machine interface based on TwinCAT software for PLC control. The advantage of this software is its built-in TwinCAT scope2 function, which simulates an oscilloscope to enable real-time waveform recording of any variable in the program.

The master controller is a PLC with the following functions: it communicates with six slave controllers via EtherCAT industrial Ethernet, receiving uploaded data including six bridge arm currents, DC-side voltage, three-phase output voltage and current, and individual sub-module capacitor voltages, while issuing corresponding bridge arm modulation wave signals to the slave controllers. As the core for MMC system computation and control, the master controller primarily implements the outer power loop, inner current loop, and circulating current suppression control, generating modulation waves for distribution to each slave controller.

The slave controllers adopt a set of EtherCAT slave devices developed by Beckhoff, based on the slave interface controller ET1100 and DSP chip TMS320F28335. Their main functions are as follows: they sample three-phase MMC upper and lower bridge arm currents, DC-side voltage, and three-phase output voltage and current through A-D modules and upload this data to the master PLC; they receive corresponding bridge arm modulation wave signals from the master station while also receiving sub-module capacitor voltage, capacitor current, and fault signals, and generate PWM signals for distribution to respective sub-modules. The slave controllers are responsible for MMC system modulation control and capacitor voltage balancing control. It should be noted that there are six EtherCAT slave devices in total. To conserve resources, each device handles signal processing for four sub-modules—i.e., one bridge arm. For future level number expansion, the number of sub-modules controlled by each EtherCAT slave device can be set to less than or equal to four, provided that the total number of cascaded sub-modules per bridge arm divided by the number of slave controllers per bridge arm equals an integer. This approach both reduces cost and increases system structural flexibility.

Additionally, the experimental platform includes 32 functional boards: one A-D board, one three-phase main circuit board, six signal adapter boards, and 24 sub-boards. The A-D board connects to the three-phase main circuit board, responsible for sampling bridge arm currents, DC bus voltage, and MMC AC-side output voltage and current, as well as hardware fault protection, sending sampled values via signal adapter boards to the EtherCAT slave devices. The signal adapter boards classify three-phase sampling signals by phase and distribute them to the EtherCAT slave devices responsible for controlling each phase, while also sending PWM signals from each slave controller to respective sub-modules after isolation. The sub-boards include individual H-bridge main circuit modules, sub-module capacitor voltage and current sampling and protection modules, and driver circuits. A sample board is shown in [Figure 5a: see original paper]. [Figure 5b: see original paper] shows the physical diagram of one phase of the MMC experimental system. In the figure, the PLC is on the left, the middle section shows the slave controller connected via a signal adapter board to four sub-modules forming one phase's upper arm, and the right section similarly shows the lower arm of one phase.

## 4 Synchronization Issues and Implementation

Since each bridge arm uses a separate controller with independent clocks and PWM transmitters, clock synchronization issues arise between upper and lower arms of the system and between different phases [13]. [Figure 6: see original paper] illustrates the serious consequences of asynchronization. Assuming each of the upper and lower arms of one phase has four modules, the states of each module in the previous switching period are shown in the left half of [Figure 6a: see original paper], with the next period assumed to output a zero-level state. Ideally, all modules would synchronously enter the next period. However, if the lower arm enters the next period with a delay of T, as shown in the right half of [Figure 6a: see original paper], sub-modules 7 and 8 that should be in the off-state become conducting, causing the phase to output a 1-level voltage during period T and resulting in a level jump. The most severe consequence of clock asynchronization occurs when all sub-modules of a phase are in the cut-off state during period T, effectively applying the entire DC-side voltage across the inductor. From Equation (1), this causes circulating current to rise rapidly, potentially damaging devices. [Figure 6b: see original paper] shows the equivalent circuit diagram of one phase during this period T.

The EtherCAT industrial Ethernet technology employed in this system features a built-in distributed clock function. When using DC synchronization mode, the first slave with synchronization capability is designated as the reference clock by default, which synchronizes other devices and the master clock. During operation, the distributed clock control unit of the slave ESC chip generates a synchronization signal Sync0. The Sync0 signal is normally high and periodically generates a short low-level pulse. When the Sync0 signal transitions from high to low, an interrupt event is generated that resets the time base counter

value used for generating the carrier signal to zero in the interrupt subroutine.

The period of the synchronization signal Sync0 can be set equal to the carrier period or an integer multiple thereof. The synchronization mode schematic is shown in [Figure 7a: see original paper]. To verify the clock synchronization function, the master PLC sends identical modulation waves to three slaves, with the slave controller carrier frequency set to 5 kHz. Without the synchronization clock function, the PWM signals generated by the three slaves are shown in [Figure 7b: see original paper], where offsets exist between PWM signals from different slaves with varying offset times, proving slave controller clock asynchronization. When the synchronization clock function is enabled, the PWM signals generated by the three slaves are shown in [Figure 7c: see original paper] and [Figure 7d: see original paper], where the offset time between PWM signals from each slave is 1.4 ns—negligible—proving precise synchronization among slaves.

The experiment employs direct modulation and sub-module voltage sorting methods. [Figure 8a: see original paper] shows the A-phase output voltage waveform without the synchronization clock function. Zooming in on one period of the voltage waveform reveals a level jump at point A. [Figure 8b: see original paper] shows the A-phase output voltage waveform with the synchronization clock function enabled. Zooming in on one period shows that the level jump phenomenon is effectively eliminated.

## 5.2 Closed-Loop Test

[Figure 9a: see original paper] and [Figure 9b: see original paper] show the three-phase output voltage and current waveforms, respectively. [Figure 9a: see original paper] demonstrates that the MMC three-phase output voltage consists of finely structured nine-level combinations, forming a nine-level circuit. [Figure 9b: see original paper] shows that the output current is relatively smooth, approximating a 50 Hz sinusoidal wave. [Figure 9c: see original paper] displays the A-phase upper and lower arm currents and circulating current waveforms, revealing that the arm currents contain DC and fundamental components plus a second harmonic component, which can be filtered using circulating current suppression strategies. [Figure 9d: see original paper] shows the sub-module capacitor voltage waveforms, demonstrating stable capacitor voltage around 25 V and effective voltage balancing implementation. The MMC operating conditions shown in [Figure 9: see original paper] confirm that the designed EtherCAT-based modular multilevel converter control system is feasible and precisely achieves synchronization among modules. Direct modulation and capacitor voltage balancing strategies can be effectively implemented on this hardware platform.

# 6 Conclusion

This paper first addresses the problems existing in modular multilevel converter systems by designing an EtherCAT-based MMC control system scheme. This

system effectively reduces control complexity, improves transmission rate and reliability between master and slave stations, and utilizes the distributed clock function to achieve precise carrier signal synchronization among slave controllers, enhancing the scalability of MMC modular cascades. Based on this control system, the entire experimental platform' s hardware architecture was designed. Finally, direct modulation and capacitor voltage sorting algorithms were applied to three-phase MMC experiments, with results verifying the effectiveness of the proposed scheme.

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*Note: Figure translations are in progress. See original paper for figures.*