Voltage Balancing Strategy for Single-Phase Multilevel Inverters Based on SVPWM Technology (Postprint)

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Abstract

Multilevel inverters exhibit the problem of DC-side voltage imbalance in voltage-dividing capacitors, which can cause distortion of output voltage and current waveforms, degrade circuit performance or lead to loss of system control, and even result in a reduction of the number of levels, thereby forfeiting many inherent advantages of multilevel inverters. This paper analyzes the DC-side voltage imbalance issue in single-phase three-level forward-isolated inverters and proposes a voltage balancing strategy based on single-phase SVPWM technology. This strategy does not increase the complexity of the original inverter topology; it achieves voltage balancing of the dividing capacitors by merely incorporating a decision-making component into the SVPWM control. Finally, the reliability of the proposed voltage balancing strategy is verified through simulation experiments conducted in the Power Simulation environment.

Full Text

Research on Capacitor Voltage Balancing Strategy for Single-Phase Multi-Level Inverters Based on SVPWM Technology

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Abstract

DC capacitor voltage unbalance in multi-level inverters causes distortion of output voltage waveforms and degeneration of voltage levels. This issue is analyzed for single-phase three-level inverters, and a voltage balancing control strategy based on single-phase SVPWM is proposed. This control strategy realizes voltage balancing without any auxiliary circuit by appropriately selecting switching patterns and determining their duration. The reliability and validity of the proposed control strategy have been verified through simulation results carried out in the Power Simulation environment.

Keywords: Voltage balancing strategy, multi-level inverter, single-phase SVPWM

Author Biographies

Guan Yue (female, born 1991) is a Ph.D. candidate whose research interests include power electronics and smart grids.

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1 Introduction

DC capacitor voltage unbalance in inverter circuits causes distortion of output voltage and current waveforms, deteriorates circuit performance, and can even lead to system 失控 [1-2]. This imbalance results in a reduction of voltage levels, causing multi-level inverters to lose their inherent advantages. For the DC-side voltage balancing problem in single-phase three-level inverters, two main solutions exist [3-7]: The first involves adding hardware circuits, such as increasing capacitor values or paralleling high-power resistors. While simple and effective, this approach reduces power density. The second solution modifies control methods, such as filtering DC components from the modulation wave or monitoring capacitor voltage for feedforward control, which increases circuit complexity.

Benefiting from SVPWM technology, three-phase inverter power systems have achieved excellent control performance [8-11]. This paper applies SVPWM technology to single-phase inverter systems to obtain similar effects. Based on theoretical analysis of neutral-point voltage deviation, a voltage balancing strategy using single-phase SVPWM control is proposed. By simply adding a selection component to the control method and choosing appropriate switching voltage vectors and their durations, the voltage balancing objective can be effectively achieved without increasing circuit complexity.

2 Single-Phase SVPWM Voltage Balancing Principle

This section explains the voltage balancing principle using a single-phase three-level inverter bridge as an example. The inverter topology is shown in [Figure 1: see original paper]. Sa and Sb represent the switching states of phases a and b, respectively, and can take values of 1, 0, or -1, corresponding to potentials at points a or b of Udc/2, 0, and -Udc/2. When the two phases operate in different switching states, five different potential differences Uab exist between points a and b, which are classified into five voltage vectors based on their magnitude, as listed in .

Assuming the DC voltage source is constant, the voltage deviation between the two dividing capacitors can be analyzed. The sum of the shifts is zero, and the two voltage-dividing capacitors have equal capacitance values, both being C. Considering the relationship between capacitor voltage and current, we have:

$$i_{c1} + i_{c2} = C\left(\frac{dU_{c1}}{dt} + \frac{dU_{c2}}{dt}\right) = 0$$

According to the capacitor energy formula, the total DC-side capacitor offset energy is:

$$\Delta = \frac{C}{2}(U_{c1}^2 + U_{c2}^2) - \frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2$$

where Uc is the neutral-point voltage of the two DC-side voltage-dividing capacitors. It can be seen that Δ 0, and the larger this value, the greater the total offset. To achieve voltage balancing, Δ must be made to decrease. The rate of change is:

$$\frac{d\Delta}{dt} = C\left(U_{c1}\frac{dU_{c1}}{dt} + U_{c2}\frac{dU_{c2}}{dt}\right) = U_{c1}i_{c1} + U_{c2}i_{c2} = i_1\left(U_c - \frac{U_{dc}}{2}\right)$$

where Uc can be obtained by sampling the neutral-point voltage value.

For the charging current, considering the small number of levels (only three levels), the relative current magnitude under different switching states can be obtained through qualitative analysis without monitoring the topology current. Using the transformer primary inductor current iN1 in [Figure 1: see original paper] as a reference, the relationship between capacitor charging current and iN1 under different switching states is analyzed, as shown in .

Only 1/2 vectors (V2, V3) affect the neutral-point voltage when acting, while zero vectors and full vectors are balance-independent vectors. By selecting appropriate redundant vectors, voltage balancing can be achieved while maintaining the output voltage unchanged. When synthesizing the target vector, simply selecting voltage vectors that satisfy dΔ/dt 0 will achieve the voltage balancing objective.

Considering that switching state transitions may increase harmonic losses, this paper adopts symmetric segmented control, as shown in [Figure 3: see original paper]. In regions one and four, the sequence of 1/2 vector, 1 vector, 1 vector, and 1/2 vector is used. In regions two and three, the sequence of zero vector, 1/2 vector, zero vector, zero vector, 1/2 vector, and zero vector is used. Based on the comparison between the sampled neutral-point voltage and the theoretical value, the required polarity of i1 is determined, and the corresponding switching state is directly selected. By continuously selecting the optimal vector during the process of synthesizing the required voltage vector, the voltage balancing objective can be achieved.

4 Simulation Results and Analysis

SVPWM control is originally used in three-phase power systems. By analogy, the single-phase SVPWM control principle can be obtained. Five voltage vectors of different lengths divide the two-dimensional plane into four regions. By introducing a virtual rotating vector that starts from the asterisk on the negative -axis in [Figure 2: see original paper] and rotates counterclockwise, its projection V on the -axis becomes the desired voltage vector to be synthesized:

$$V = 2U_{\phi} \sin(\omega t)$$

By comparing V with the magnitudes of various voltage vectors, the region where it resides can be determined. The desired voltage vector can then be synthesized using the two voltage vectors in that region with appropriately set durations.

To verify the correctness of the proposed voltage balancing strategy, a Power Simulation model was built with the following key parameters: DC source of 220V, DC-side dividing capacitor value of 220 F, output filter inductor of 150 H, output filter capacitor of 125 F, and load resistance of 10Ω. The modulation index M was set to 0.8.

Without the proposed voltage balancing strategy, the topology may experience a condition where one capacitor continuously discharges until its voltage reaches zero, causing the three-level inverter to degenerate into a two-level inverter, as shown in [Figure 4: see original paper]. This demonstrates that the DC-side voltage balancing problem in multi-level inverters not only affects output voltage quality but also leads to level number degradation, causing the multi-level topology to lose its inherent advantages.

[Figure 5: see original paper] shows the voltage waveforms before the filter and across the dividing capacitors after applying the proposed single-phase multi-level inverter SVPWM voltage balancing strategy. The results demonstrate that the strategy ensures a perfect three-level output, with the two dividing capacitor voltages maintained at approximately Udc/2, verifying the correctness of the proposed strategy.

[Figure 6: see original paper] presents the voltage waveforms of the two DC-side dividing capacitors, with maximum and minimum values marked as 110.567V and 109.431V, respectively. These deviate from the theoretical value of 110V by only 0.51% and 0.39%.

[Figure 7: see original paper] illustrates the regulation effect of the proposed voltage balancing strategy on the two dividing capacitor voltages. When one dividing capacitor acts as a voltage source in the circuit, its voltage inevitably decreases. The control circuit then selects switching vectors that drive the neutral-point voltage toward Udc/2 to regulate the two capacitor voltages, causing them to fluctuate within a small range around the theoretical value. The filtered voltage waveform is shown in [Figure 8: see original paper], demonstrating the effectiveness of the proposed voltage balancing control method.

[Figure 9: see original paper] presents the FFT analysis of the output voltage waveform, showing that the voltage balancing strategy achieves voltage balancing without degrading the output voltage waveform quality.

5 Conclusion

The DC-side capacitor voltage unbalance problem in multi-level inverters not only affects output waveforms but also causes level number degradation, leading to loss of multi-level advantages. The proposed single-phase SVPWM-based voltage balancing strategy simply and effectively solves the DC-side voltage imbalance problem in single-phase three-level inverters by selecting appropriate switching vectors and their durations in each switching cycle. This approach is practical and generalizable.

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