# Neutral-Point Potential Balance Control Method for Three-Level Inverters Based on Discontinuous Pulse Width Modulation (Postprint)

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**Date:** 2019-03-05T00:00:00+00:00

## Abstract

In medium-voltage high-power inverters, issues such as high switching frequency and significant switching losses exist. The adoption of Discontinuous Pulse Width Modulation (DPWM) strategy can reduce switching frequency while mitigating switching losses. Typically, conventional neutral point balancing methods introduce compensation voltage into the reference voltage; however, when employing DPWM modulation, the existence of intervals between switch turn-on and turn-off prevents conventional balancing methods from achieving effective neutral point balance control. This paper first analyzes the causes of neutral point imbalance, subsequently examines the limitations of traditional balancing control methods, and finally proposes a discontinuous pulse width angle adjustment control method. This approach ensures low switching frequency while achieving neutral point voltage balance, without requiring additional hardware circuits or complex computational methods. The effectiveness of the proposed method is finally validated through Matlab/Simulink simulation.

## Full Text

## A New Discontinuous PWM Method for Three-Level Inverter Neutral-Point Voltage Balancing Control

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### Abstract

In medium-voltage high-power inverters, high switching frequency leads to significant switching losses. Discontinuous pulse-width modulation (DPWM) strategies can reduce both switching frequency and losses. Conventional neutral-point balancing methods typically inject a compensation voltage into the reference voltage, but these approaches fail under DPWM because the fixed intervals between switching actions prevent effective neutral-point control. This paper first analyzes the causes of neutral-point voltage imbalance and the limitations of traditional balancing methods, then proposes a novel discontinuous pulse-width angle adjustment control method. This approach maintains low switching frequency while achieving neutral-point voltage balance without requiring additional hardware or complex calculations. Matlab/Simulink simulations validate the effectiveness of the proposed method.

**Keywords:** Three-level inverter, discontinuous pulse width modulation, neutral-point voltage balancing

## 1 Introduction

Multilevel inverter topologies include T-type, diode-clamped, and H-bridge configurations. These inverters offer advantages such as low output voltage harmonic content, small voltage change rates, and reduced EMI, making them essential for medium-voltage high-power applications [1]. The diode-clamped three-level inverter is the most widely used topology in industrial applications, offering the key benefits of requiring no independent clamping capacitors or transformers, simple hardware structure, and reduced inverter volume, making it a promising configuration [2]. As energy efficiency becomes increasingly critical, improving power conversion efficiency has emerged as a major research focus. Compared with continuous pulse-width modulation (CPWM), discontinuous pulse-width modulation (DPWM) can significantly reduce switching losses by maintaining certain switches in a non-switching state during specific intervals of the fundamental voltage period [3]. However, these non-switching intervals cause substantial neutral-point voltage fluctuations under DPWM, which degrade output current and voltage quality, necessitating effective suppression of neutral-point voltage variation.

Numerous studies have proposed DPWM strategies for three-level inverters. For instance, reference [4] utilizes two zero vectors (000 and 111) alongside other non-zero vectors to create 60° non-switching intervals at both the positive and negative peaks of the output voltage, known as the DPWM1 strategy. Reference [5] employs only one zero vector (000 or 111) to achieve 120° non-switching intervals in either the negative or positive half-cycle, designated as DPWMMIN and DPWMMAX. References [6-7] introduce three additional DPWM strategies: DPWM0, which advances the two 60° non-switching intervals by 60° relative to the voltage peaks; DPWM2, which delays them by 30°; and DPWM3, which implements 30° non-switching intervals every 60° for switches in the same bridge arm. These works primarily focus on modulation principles and switching sequence optimization, or compare performance metrics among select DPWM methods. Other research concentrates on DPWM applications, such as reference [8] discussing DPWM implementation in active power filters.

Building upon these studies, this work adopts the DPWM1 modulation method and proposes a novel neutral-point potential balancing control strategy for NPC three-level inverters operating under DPWM. By evaluating the initial conditions and selecting an optimal adjustment angle, the method regulates the width of discontinuous pulse-width intervals in both positive and negative half-cycles to achieve neutral-point balance. This approach requires no additional hardware or complex algorithms—only a simple regulator to calculate the optimal adjustment angle—offering flexible, straightforward control suitable for digital implementation.

## 2.1 Operating Principle of Neutral-Point-Clamped Three-Level Inverters

The switching states for active devices in a three-level NPC inverter are summarized in Table 1 . For phase A, switching state P indicates that the two upper switches conduct, yielding a terminal voltage U_AZ = +U_dc/2 relative to the neutral point Z. State N indicates the two lower switches conduct, giving U_AZ = -U_dc/2. State O indicates the two middle switches conduct, where clamping diodes hold U_AZ at zero potential. The load current direction determines which diode conducts. As shown in Table 1, switches S_a1 and S_a3 operate complementarily—when one is on, the other must be off. Similarly, S_a2 and S_a4 operate in a complementary fashion. The NPC three-level inverter topology is illustrated in Figure 1 [Figure 1: see original paper].

Considering all three phases, the inverter has 27 possible switching state combinations corresponding to 19 distinct voltage vectors, with their space vector diagram shown in Figure 2 [Figure 2: see original paper]. Based on magnitude, these vectors are classified into four groups: zero vectors, small vectors, medium vectors, and large vectors [9]. The relationship between switching states and voltage vectors is provided in Table 2 . As evident from Table 2 and Figure 2, each voltage vector may correspond to multiple switching states, with redundant states increasing toward the inner layers of the diagram [10].

## 2.2 Causes of Neutral-Point Potential Imbalance

Figure 3 [Figure 3: see original paper] illustrates how switching states affect neutral-point voltage. Zero and large vectors have no impact on the neutral-point potential because the neutral point remains floating, as shown in Figure 3a. Figure 3b depicts the inverter operating in P-type small vector state POO, where the three-phase load connects between the positive DC bus and neutral point. Current flowing into the neutral point charges capacitor C1, causing U_dc1 > U_dc2 and raising the neutral-point voltage. Thus, P-type small vectors increase the neutral-point potential. Conversely, Figure 3c shows the N-type small vector ONN, where the load connects between the negative DC bus and neutral point. Current entering the neutral point charges capacitor C2, causing U_dc1 < U_dc2 and lowering the neutral-point voltage.

Medium vectors also affect the neutral-point potential, as shown in Figure 3d for state PON, where phases A, B, and C connect to the positive bus, neutral point, and negative bus, respectively. Depending on the operating conditions of the motor load, either the upper or lower capacitor may charge, making the neutral-point current direction unpredictable and allowing the neutral-point potential to either rise or fall. Therefore, the effect of medium vectors on neutral-point potential cannot be determined. As shown in Figure 3e, zero and large vectors have no influence on neutral-point voltage since the neutral point remains isolated.

The structural characteristics of NPC three-level inverters cause the output terminal of each phase to connect to the DC-link capacitor neutral point during certain switching states, allowing current to flow into or out of the series capacitor midpoint. This creates unbalanced charging and discharging, leading to continuous neutral-point potential variation. The primary causes of neutral-point potential imbalance include [11-12]: (1) manufacturing tolerances preventing perfect capacitor parameter matching, resulting in uneven charging; (2) switching delays; and (3) power factor effects—reactive current components cause periodic neutral-point voltage fluctuations, while active current components cause offset that accumulates over time. Neutral-point imbalance degrades grid-connected inverter output voltage waveforms, exacerbates imbalance, damages switching devices, and reduces capacitor lifespan through continuous cycling. Therefore, neutral-point balancing control is critical.

The analysis reveals that neutral-point potential offset primarily results from neutral-point current at any given instant, with imbalance arising from differences in the magnitude and duration of currents flowing into and out of the neutral point. Consequently, neutral-point voltage balance can be achieved by controlling these currents within small time intervals.

## 3.1 Traditional Control Method

Conventional neutral-point balancing injects a compensation voltage into the reference voltage to alter small vector duty times. If the upper capacitor voltage is lower than the lower capacitor voltage, a negative half-cycle compensation voltage is added to balance the neutral point. This reduces the duration of P-state small vector PPO and increases N-state small vector OON, as shown in Figure 4 [Figure 4: see original paper], causing the lower capacitor voltage to decrease and the upper capacitor voltage to increase. Conversely, adding a positive half-cycle compensation voltage increases P-state small vector duration while decreasing N-state duration.

## 3.2 Limitations of Traditional Methods Under DPWM

When neutral-point imbalance occurs under DPWM1 modulation, traditional control methods cannot achieve balance. If the upper capacitor voltage exceeds the lower capacitor voltage, a positive half-cycle compensation voltage is injected to increase P-state small vector duration and reduce N-state duration. Under conventional PWM, neutral-point current flowing out decreases as P-state duration increases. However, under DPWM, injecting compensation voltage cannot alter the duty time of clamped small vectors because each phase has clamped intervals, so the outgoing neutral-point current does not decrease.

The seven-segment switching sequence contains pairs of small vectors with opposite effects on neutral-point potential, enabling balance control through adjustment of positive and negative small vector durations. However, under DPWM1, the N-state small vectors NOO, ONO, and OON are separated by 60° intervals. Although compensation voltage modifies reference voltage, the resulting small vector time adjustments are insufficient to balance the neutral-point voltage. In DPWM strategies, only one phase is clamped during each fundamental period. Injecting excessive compensation voltage may cause discontinuous pulse-width intervals to overlap other phases, leading to output current distortion. Consequently, traditional balancing methods prove ineffective under DPWM modulation.

## 3.3 Discontinuous Pulse-Width Angle Adjustment Control Method

The proposed method adjusts the widths of discontinuous pulse-width intervals in opposite proportion between positive and negative half-cycles while maintaining fixed clamping angles, thereby modifying small vector durations. Extending the positive half-cycle clamping interval increases P-state duration and P-type small vector action time while shortening the negative half-cycle clamping interval reduces N-state small vector duration. Conversely, extending the negative clamping interval increases N-type small vector duration while decreasing P-type duration.

This inverse proportional adjustment ensures constant clamping angle per cycle, reduces switching losses, and prevents overlap between discontinuous intervals of different phases.

The capacitor voltage difference is defined as V_x(k), its previous value as V_x(k-1), and the tolerance threshold as |V_n|. If |V_x(k)| < |V_n|, the neutral point is considered balanced. The adjustment rules are divided into two main scenarios, each containing four cases, with the adjustment angle updated according to:

(k) = (k-1) ± Δ

where (k) is the current angle, (k-1) is the previous angle, and Δ is the adjustment step. The appropriate value is determined as follows:

**Scenario 1: V_dc1 > V_dc2** (adjust to increase positive half-cycle discontinuous width while decreasing negative half-cycle width) 1. If V_x(k) > 0 and V_x(k) V_x(k-1), the deviation is increasing, so (k) = (k-1) + Δ . 2. If V_x(k) > 0 and V_x(k) < V_x(k-1), the voltage difference is decreasing but still present, so  (k) =  (k-1) + Δ . 3. If V__x(k) > 0 and V__x(k) < V__x(k-1), the system has overshot the balance point due to excessive positive clamping and insufficient negative clamping, so  (k) =  (k-1) - Δ . 4. If |V__x(k)| < |V__n|, neutral-point balance is achieved, so  (k) =  (k-1).

**Scenario 2: V__dc1 < V__dc2** (adjust   to increase negative half-cycle discontinuous width while decreasing positive half-cycle width) 1. If V__x(k) < 0 and V__x(k)   V__x(k-1), the deviation is increasing, so  (k) =  (k-1) + Δ . 2. If V__x(k) < 0 and V__x(k) > V__x(k-1), the voltage difference is decreasing but still present, so  (k) =  (k-1) + Δ . 3. If V__x(k) < 0 and V__x(k) < V__x(k-1), the system has overshot the balance point due to excessive negative clamping and insufficient positive clamping, so  (k) =  (k-1) - Δ . 4. If |V__x(k)| < |V__n|, neutral-point balance is achieved, so  (k) =  (k-1).

The flowchart for determining the proper   adjustment is shown in Figure 5 [Figure 5: see original paper].

## 4 Simulation and Results Analysis

Matlab/Simulink simulations verify the proposed neutral-point balancing control method. A three-level inverter module was constructed with an RL load. Simulation parameters include: DC source voltage: 140 V; DC-link capacitors: 1100  F each; load resistance: 10 Ω; load inductance: 1.5 mH; reference current: sinusoidal waveform with 13 A amplitude and 50 Hz frequency; sampling period: 100  s; tolerance threshold |V__n| = 1 V.

Figure 6 [Figure 6: see original paper] shows the phase voltage and reference voltage waveforms using the traditional control method, while Figure 7 [Figure 7: see original paper] presents the results with the proposed method. Each phase reference voltage is clamped for 60°, during which the output phase voltage remains constant. Due to capacitor voltage differences, the positive and negative half-cycle peaks have different magnitudes, causing output current distortion. The traditional method adjusts the widths of positive and negative half-cycle discontinuous intervals to regulate neutral-point voltage, increasing the positive half-cycle clamping duration while shortening the negative half-cycle portion.

The DC-link capacitor voltage waveforms under the traditional method are shown in Figure 8 [Figure 8: see original paper]. With the proposed method, the two capacitor voltages gradually converge toward the neutral point with minimal fluctuation, as shown in Figure 9 [Figure 9: see original paper], demonstrating successful neutral-point balancing through discontinuous pulse-width adjustment. The output phase current, shown in Figure 10 [Figure 10: see original paper], exhibits excellent performance with a clear three-level operation pattern and near-sinusoidal waveform.

## 5 Conclusion

This paper proposes a neutral-point balancing strategy specifically designed for DPWM modulation. Due to the inherent intervals between switching actions in DPWM, conventional neutral-point balancing methods cannot achieve effective control. The proposed method adjusts small vector durations by regulating discontinuous pulse-width intervals in opposite proportion between positive and negative half-cycles, simultaneously achieving neutral-point control and maintaining low switching frequency. This approach introduces neither complex calculations nor additional hardware. Simulation results confirm the feasibility and effectiveness of the proposed method.

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*Note: Figure translations are in progress. See original paper for figures.*