Postprint: A Phase-Locking Method for Unbalanced Voltage Using Second-Order Generalized Integrator within SRF-PLL Loop

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Abstract

Grid-connected power electronic converters require precise real-time detection of grid voltage phase to achieve synchronization. For synchronous rotation transformation phase-locked methods, when three-phase grid voltage is unbalanced, the d-axis and q-axis components after Park transformation contain double-frequency disturbances, causing inaccurate phase deviation information and resulting in steady-state errors in the detected phase of the positive-sequence component. This paper analyzes the band-pass characteristics, parameter selection principles, and digital implementation methods of the second-order generalized integrator (SOGI), and applies it within the phase-locked loop for double-frequency detection. Through decoupling, the DC component in the phase detector is indirectly separated while other higher-order harmonic components are attenuated. Additionally, considering the system' s dynamic performance and disturbance rejection capability, a parameter design procedure for the loop filter based on second-order optimization in the s-domain is presented. Matlab/Simulink digital simulation results demonstrate that the phase detection steady-state error is zero under unbalanced grid voltage conditions. Finally, the algorithm is implemented on an experimental platform using a TMS320F28335 controller, and test waveforms verify the practical feasibility of the proposed method.

Full Text

SRF-PLL with In-Loop Second Order Generalized Integrator for Unbalanced Voltage Phase Locking

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Abstract

Grid-connected power electronic converters require precise real-time detection of grid voltage phase to achieve synchronization. When three-phase grid voltages become unbalanced, the d-axis and q-axis components after Park transformation contain double-frequency disturbances, which cause ripple in the phase detector of Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) and lead to steady-state error in the detected positive-sequence phase angle. This paper analyzes the band-pass characteristics, parameter selection principles, and digital implementation of the Second Order Generalized Integrator (SOGI). By applying SOGI within the PLL loop for double-frequency detection, the DC component in the phase detector is indirectly separated through decoupling while other high-order harmonic components are attenuated. Additionally, considering the trade-off between system dynamics and disturbance rejection, a loop filter parameter design procedure in the s-domain based on second-order optimum principles is presented. Matlab/Simulink digital simulation results demonstrate zero steady-state phase detection error under unbalanced voltage conditions. Finally, the algorithm is implemented on a TMS320F28335 controller-based experimental platform, with test waveforms verifying the practical feasibility of the proposed method.

Keywords: Phase-locked loop, unbalanced voltages, SOGI, detector, digital signal processor

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1 Introduction

Real-time detection of grid voltage phase is a fundamental technology, and a high-precision, fast phase-locked synchronization loop is crucial for the control of grid-connected power equipment. The Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) represents a practical solution, consisting of three main components: a phase detector that uses Park transformation to detect phase deviation from three-phase voltage signals, a loop filter PI regulator that removes high-frequency components from the phase error, and an integrator-type oscillator that calculates phase information using the steady-state error value. Through continuous closed-loop adjustment until the error becomes constant, the output signal tracks the input signal in real time. Under symmetrical and balanced three-phase grid voltage conditions, the phase detector output is a DC component that accurately reflects phase deviation information. By designing appropriate loop filter parameters, the SRF-PLL can be made a high-bandwidth system achieving sufficient steady-state accuracy and fast dynamic response. However, actual grid systems frequently experience voltage unbalance due to asymmetric loads and their dynamic characteristics. In such cases, the SRF-PLL synchronization loop tracking the positive-sequence component phase exhibits steady-state error.

To eliminate this steady-state error, one approach is to appropriately reduce the PLL system bandwidth to enhance its disturbance rejection capability, though this compromises dynamic response. An alternative solution involves applying various types of filters either inside or outside the SRF-PLL loop to obtain accurate phase angle deviation information through additional filtering, thereby reducing or eliminating steady-state error. This paper introduces an in-loop filtering scheme for SRF-PLL utilizing a Second Order Generalized Integrator (SOGI) to address voltage unbalance. The paper first analyzes the characteristics of the phase detector output signal under unbalanced conditions, then provides a detailed discussion of SOGI' s band-pass characteristics and its digital implementation. Digital simulation results demonstrate that SOGI effectively improves phase-locking performance under unbalanced voltage conditions while also accommodating certain levels of harmonic pollution. Finally, the proposed method is implemented on a TMS320F28335 controller-based experimental platform, with test waveforms confirming its excellent performance.

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2 SRF-PLL Phase Detector Output Signal Under Unbalanced Voltage

Ignoring zero-sequence components, unbalanced three-phase voltages can be expressed as:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = V^+ \begin{bmatrix} \cos(\omega t + \phi^+) \\ \cos(\omega t + \phi^+ - \frac{2\pi}{3}) \\ \cos(\omega t + \phi^+ + \frac{2\pi}{3}) \end{bmatrix} + V^- \begin{bmatrix} \cos(\omega t + \phi^-) \\ \cos(\omega t + \phi^- + \frac{2\pi}{3}) \\ \cos(\omega t + \phi^- - \frac{2\pi}{3}) \end{bmatrix}$$

where V^+ is the positive-sequence component magnitude, V^- is the negative-sequence component magnitude, ϕ^+ and ϕ^- are initial phases, and $\omega = 2\pi \times 50\text{rad/s}$ is the fundamental angular frequency.

Applying Clark transformation to equation (1):

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = V^+ \begin{bmatrix} \cos(\omega t + \phi^+) \\ \sin(\omega t + \phi^+) \end{bmatrix} + V^- \begin{bmatrix} \cos(\omega t + \phi^-) \\ -\sin(\omega t + \phi^-) \end{bmatrix}$$

Applying Park transformation to equation (2):

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = V^+ \begin{bmatrix} \cos[(\omega-\hat{\omega})t + (\phi^+ - \hat{\phi}^+)] \\ \sin[(\omega-\hat{\omega})t + (\phi^+ - \hat{\phi}^+)] \end{bmatrix} + V^- \begin{bmatrix} \cos[(\omega+\hat{\omega})t + (\phi^- + \hat{\phi}^+)] \\ -\sin[(\omega+\hat{\omega})t + (\phi^- + \hat{\phi}^+)] \end{bmatrix}$$

where $\hat{\theta}$ is the detected phase angle of the a-phase positive-sequence component, with $\hat{\theta} = \hat{\omega}t + \hat{\phi}^+$.

If $\omega = \hat{\omega}$ and $\phi^+ = \hat{\phi}^+$, then:

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} V^+ \\ 0 \end{bmatrix} + V^- \begin{bmatrix} \cos[2\omega t + (\phi^- + \hat{\phi}^+)] \\ -\sin[2\omega t + (\phi^- + \hat{\phi}^+)] \end{bmatrix}$$

Equation (5) shows that in the dq frame, the DC component v_{qdc} represents the positive-sequence phase deviation information with amplitude related to V^+, while the double-frequency disturbance $\{v_{d2}, v_{q2}\}$ represents the original negative-sequence component with amplitude related to V^-. To accurately detect the positive-sequence component phase using SRF-PLL under voltage unbalance, the double-frequency disturbance component v_{q2} must be filtered from the phase detection signal v_q, retaining only the DC component v_{qdc}.

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3 Second Order Generalized Integrator

Reference [6] proposed a quadrature signal generator based on the Second Order Generalized Integrator (SOGI), whose structure is shown in [Figure 1: see original paper]. The input signal v is subtracted from the output signal v', multiplied by coefficient k, and two generalized integrators implement inner-loop feedback to generate orthogonal signals.

The relationship between SOGI input and output is given by:

$$H(s) = \frac{v'(s)}{v(s)} = \frac{k\omega_0 s}{s^2 + k\omega_0 s + \omega_0^2}$$

[Figure 2: see original paper] shows the frequency response of $H(s)$ when $\omega_0 = 2 \times 2\pi \times 50\text{Hz} = 628\text{rad/s}$ and $k = \{0.3, 1, 3\}$. The response exhibits band-pass characteristics at frequency ω_0 without time delay, while completely blocking DC components. Smaller k values result in narrower passband, greater attenuation of other frequency components, and stronger selectivity.

SOGI contains two integrators. Digital implementation adopts the backward Euler method [7], with structure shown in [Figure 3: see original paper] and difference equations given by (7)-(9), requiring only multiplication and addition operations with minimal computational overhead.

$$v'(n) = v'(n-1) + \omega_0 T_s \{ke(n) - \omega_0 v'(n-1)\} \quad (8)$$

$$qv'(n) = qv'(n-1) + \omega_0 T_s v'(n) \quad (9)$$

Two band-pass SOGIs are configured within the SRF-PLL loop for detection in the dq frame. The secondary components are eliminated through subtraction, allowing only the DC component to enter subsequent modules, as shown in [Figure 4: see original paper]. To ensure strong attenuation of frequency components other than ω_0 and DC components, thereby accommodating certain harmonic pollution conditions, the k value should be as small as possible; this paper selects $k = 0.3$. Additionally, since V^+ affects PLL system dynamic performance, per-unit normalization and magnitude calculation are applied to eliminate its influence.

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4 Loop Filter Parameter Design

Assuming SOGI completely separates the DC component of phase deviation from the phase detector, the SRF-PLL approximate linearized model is shown in [Figure 5: see original paper]. The loop filter adopts a PI regulator form:

$$K_f(s) = k_p + \frac{k_i}{s}$$

where k_p and k_i are the proportional and integral gains, respectively.

The open-loop transfer function is:

$$G_{ol}(s) = \frac{k_p s + k_i}{s^2}$$

The corresponding closed-loop transfer function is:

$$G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)} = \frac{k_p s + k_i}{s^2 + k_p s + k_i}$$

Equation (12) represents a typical second-order closed-loop system with standard form:

$$G_{cl}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where:

$$k_p = 2\zeta\omega_n \quad (14)$$

$$k_i = \omega_n^2 \quad (15)$$

For this closed-loop second-order transfer function, parameter design must balance fast dynamic response and good steady-state characteristics. The second-order optimum selects a damping ratio $\zeta = 0.707$, yielding bandwidth $\omega_b \approx 2.1\omega_n$. Once ζ is determined, larger undamped natural frequency ω_n results in larger bandwidth and faster response, but excessive ω_n amplifies errors and affects the transient process [8].

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5 Digital Simulation

To verify the effectiveness of the proposed approach, a Matlab/Simulink simulation model of the system in [Figure 4: see original paper] was established. Simulation parameters are listed in the table below.

[Figure 6: see original paper] presents simulation results under unbalanced conditions. Waveforms from top to bottom are: three-phase voltages v_{abc}, v_{dq}, v_{dqdc}, frequency detection value $\hat{f} = \hat{\omega}/2\pi$, phase detection value $\hat{\theta}$, and detection error $(\theta - \hat{\theta})$. Initially, the three-phase voltage is balanced, and the system reaches steady state within approximately one fundamental period, with $v_{dqdc}^{+} = 1$ pu, $\hat{f} = 50$ Hz, and $(\theta - \hat{\theta}) = 0$. At $t = 0.05$ s, v_a suddenly increases to 1.2 pu while v_c drops to 0 pu. Consequently, v_{dq} exhibits double-frequency disturbances, which after SOGI filtering leave only DC components. Simultaneously, $\hat{f}$ shows fluctuations. For comparison, the $(\theta - \hat{\theta})$ waveform includes a dashed line showing the response of SRF-PLL without SOGI, where steady-state error is reduced from $-8°$ to $+5°$ to zero. At $t = 0.15$ s, v_a suddenly drops to 0.8 pu and v_c recovers to 0.8 pu, reducing the asymmetry and disturbance component amplitude, with steady-state error further reduced to zero and transition process lasting approximately three fundamental periods.

Table: Simulation Parameters

Parameter	Value
ω_0	$2\pi \times 50 \times 2$
T_s	0.0001 s
k	$2\pi \times 31.5$

[Figure 7: see original paper] shows simulation results under harmonic pollution conditions. At $t = 0.1$ s, 3rd, 5th, and 7th harmonics are added to v_{abc} with amplitudes of 0.3 pu, 0.2 pu, and 0.1 pu respectively (to simulate asymmetry, the 5th harmonic amplitude in phase-a is 0.6 pu). Although SOGI cannot completely eliminate high-order harmonic effects, its attenuation is significant, reducing phase detection steady-state error from ±6° to ±1.5°.

Reference [9] utilizes a notch filter in the dq frame to remove double-frequency disturbances and separate DC phase detection components, also achieving zero steady-state phase angle detection error under unbalanced grid voltage. However, the notch filter provides strong attenuation only at the notch frequency while having negligible effect on other frequencies. If grid voltage contains harmonics, v_q includes other high-order harmonic disturbance components, resulting in larger steady-state errors. [Figure 2: see original paper] demonstrates that SOGI also attenuates high-order harmonics, providing the advantage that under the same bandwidth conditions, the proposed scheme yields smaller steady-state detection errors when three-phase voltages contain harmonics. [Figure 8: see original paper] presents comparative simulation results with identical input voltages as in [Figure 6: see original paper] and [Figure 7: see original paper]. Under unbalanced conditions, both schemes achieve zero steady-state error, but under harmonic pollution, the proposed scheme' s steady-state error is ±1° compared to ±2° for the notch filter scheme.

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6 Experimental Results

To verify feasibility, the algorithm in [Figure 4: see original paper] was implemented using C language in the CCS development environment on a floating-point DSP TMS320F28335 from TI. A signal generator produced simulated grid voltages that were conditioned and fed to the DSP' s 12-bit AD module. A general-purpose timer generated 10 kHz pulses to drive interrupt routine execution, with the phase-locked algorithm running every 0.0001 s. Software operational variables were modulated onto a 150 kHz PWM wave output to GPIO ports, observed in real-time after external low-pass RC filtering with 600 Hz cutoff frequency. SOGI was implemented using equations (7)-(9). For trigonometric operations, an optimized floating-point math library from TI was incorporated for direct real-time calculation. Integral operations were discretized using the backward Euler method, and to reduce accumulation errors in high-speed operations, the PI regulator adopted an incremental structure.

[Figure 9: see original paper] presents experimental test results under unbalanced conditions, while [Figure 10: see original paper] shows results under harmonic conditions with inputs identical to simulations. The detection error curves demonstrate that in both fault conditions, the system successfully tracks the fundamental component due to SOGI' s filtering effect, with results closely matching digital simulations.

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7 Conclusions

1. Under three-phase voltage unbalance, the double-frequency disturbance in the SRF-PLL phase detector causes steady-state error in positive-sequence component phase detection.
2. When ω_0 is set to double the fundamental frequency, SOGI detection performance depends on parameter k. Smaller k values provide strong attenuation of both low-frequency and high-frequency components, enabling the proposed method to reduce phase detection steady-state error compared to conventional SRF-PLL under input voltage harmonic pollution.
3. When grid voltage frequency fluctuates, feedforward of the frequency detection value from SRF-PLL enables adaptive frequency tracking for SOGI detection.
4. When the loop filter adopts PI form, system damping ratio and undamped natural frequency are tuned using second-order optimum principles, balancing stability and speed across a wide range.
5. SOGI detection is easily implemented digitally, requiring only a few additional multiplication and addition operations. Implemented on high-speed DSP, the computational load is small and does not affect real-time performance.

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Note: Figure translations are in progress. See original paper for figures.