Common-Mode Voltage Suppression Strategy for Two-Level Voltage Source Inverters (Postprint)

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Date: 2019-03-05T00:00:00+00:00

Abstract

This paper primarily introduces several methods for suppressing inverter common-mode voltage (CMV). One category is based on optimized space vector modulation strategies, mainly including zero vector replacement (AZSPWM), nearest non-zero vector synthesis (NSPWM), virtual space vector modulation (VSVM), and other strategies. Another category suppresses common-mode voltage by modifying the hardware circuit topology, primarily through the utilization of three-phase four-leg topology. Relevant simulations and analyses are performed on these two categories of methods to provide references for research on common-mode voltage suppression schemes.

Full Text

Preamble

Research on Common Mode Voltage Suppression Strategy for Two-Level Voltage Source Inverter

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Abstract

This paper introduces several methods for suppressing the common mode voltage (CMV) of inverters, which are primarily divided into two categories. The first category involves optimization of space vector modulation strategies, including Active Zero State PWM (AZSPWM), Near State PWM (NSPWM), and Virtual Space Vector Modulation (VSVM). The second category suppresses CMV by modifying the hardware circuit topology, mainly through the use of a three-phase four-leg topology. This paper presents relevant simulations and analyses of these two approaches to provide reference for research on CMV suppression schemes.

Keywords: Inverter, Space Vector Modulation, Common Mode Voltage
Chinese Library Classification: TM464

1 Introduction

With the widespread application of frequency converters, various negative effects have become increasingly prominent. In particular, the high-frequency common mode voltage generated by converters can induce high-amplitude shaft voltage on motor shafts, creating bearing currents that accelerate motor bearing aging and cause premature failure, thereby reducing motor service life. Common mode voltage also produces significant common-mode leakage currents through stray capacitances and parasitic coupling capacitances in the system. This leakage current flows to ground through the electrostatic coupling between stator windings and the motor frame, and returns to the grid via the grounding conductor. This not only causes malfunctions in protection devices but also generates substantial common-mode electromagnetic interference that seriously affects the normal operation of other control systems or electronic equipment.

In recent years, numerous scholars have conducted extensive research on CMV suppression, which can be broadly divided into two approaches. The first approach suppresses CMV through modulation strategy optimization at the software algorithm level. With the rapid advancement of digital processor performance, inverter modulation strategy optimization has primarily focused on Space Vector Modulation (SVM) schemes, giving rise to several key modulation strategies: Active Zero State PWM (AZSPWM), Near State PWM (NSPWM), and Virtual Space Vector Modulation (VSVM). The second approach suppresses CMV by modifying the inverter’ s hardware circuit structure or peripheral components. This method primarily involves adding a filter to eliminate the generated common mode voltage. Subsequent research has upgraded this approach by adding a fourth bridge leg to construct a three-phase four-leg topology for CMV suppression. This paper provides a brief analysis of the fundamental principles of each scheme and presents simulation verification results.

2 Common Mode Voltage in Traditional Two-Level Inverters

The topology of a conventional two-level voltage source inverter is shown in [Figure 1: see original paper]. Common mode voltage is defined as the voltage between the inverter’ s output neutral point and ground reference, denoted as U_{no}. Based on the inverter topology, we have:

$$U_{no} = U_{n1} + U_{1o}$$
$$U_{no} = U_{n2} + U_{2o}$$
$$U_{no} = U_{n3} + U_{3o}$$

Since $U_{n1} + U_{n2} + U_{n3} = 0$, combining the above equations yields:

$$U_{no} = \frac{U_{1o} + U_{2o} + U_{3o}}{3}$$

Assuming the DC bus voltage of the inverter is U_{dc}, the voltage space vector distribution using traditional SVPWM control is shown in [Figure 2: see original paper]. The common mode voltage distribution for different voltage space vectors is presented in the table below.

Table: CMV of Different Switching States

S1, S3, S5 State	Common Mode Voltage U_{no}
000	$-U_{dc}/2$
100	$-U_{dc}/6$
110	$U_{dc}/6$
010	$-U_{dc}/6$
011	$U_{dc}/6$
001	$-U_{dc}/6$
101	$U_{dc}/6$
111	$U_{dc}/2$

When the reference voltage vector U_{ref} is in Sector I, the traditional SVPWM vector synthesis scheme employs vectors $U_0(000)$, $U_1(100)$, $U_2(110)$, and $U_7(111)$. The switching sequence and CMV distribution are shown in [Figure 3: see original paper].

As shown in [Figure 3: see original paper], the traditional SVPWM modulation strategy produces a CMV peak of $U_{dc}/2$. However, by avoiding zero vectors in the voltage vector selection, the CMV peak can be reduced to $U_{dc}/6$, leading to various optimized SVM-based modulation strategies.

3 Modulation Strategies for CMV Suppression

3.1 Active Zero State PWM (AZSPWM)

The fundamental principle of AZSPWM is to replace zero voltage vectors with two opposite non-zero voltage vectors. The space vector distribution is shown in [Figure 4: see original paper]. When the reference voltage vector U_{ref} is in Sector I, the AZSPWM vector synthesis scheme employs vectors $U_6(101)$, $U_1(100)$, $U_2(110)$, and $U_3(010)$. The switching sequence and CMV distribution are shown in [Figure 5: see original paper].

As shown in [Figure 5: see original paper], the AZSPWM modulation strategy effectively limits the CMV peak to $U_{dc}/6$, which is only one-third of that produced by conventional SVPWM control.

3.2 Near State PWM (NSPWM)

The fundamental principle of NSPWM is to synthesize the reference vector using the three nearest non-zero vectors. The space vector distribution is shown in [Figure 6: see original paper]. When the reference voltage vector U_{ref} is in Sector I, the NSPWM vector synthesis scheme employs vectors $U_6(101)$, $U_1(100)$, and $U_2(110)$. The switching sequence and CMV distribution are shown in [Figure 7: see original paper].

Similar to AZSPWM, this scheme can reduce the CMV peak to $U_{dc}/6$. Moreover, within one switching period T_s, the CMV polarity changes only 4 times, fewer than the 6 times in AZSPWM, resulting in fewer harmonic components.

3.3 Virtual Space Vector Modulation (VSVM)

The fundamental principle of VSVM is to synthesize the reference voltage vector using synthesized virtual space vectors that have zero common mode voltage. The space vector distribution is shown in [Figure 8: see original paper], where the reference vector U_{ref} is synthesized through the action of virtual space vectors U_{61} and U_{12}, along with two real vectors U_6 and U_3. The virtual space vectors U_{61} and U_{12} correspond to zero CMV (as an average value). The switching sequence and CMV distribution are shown in [Figure 9: see original paper].

As shown in [Figure 9: see original paper], the VSVM scheme also reduces the CMV peak to $U_{dc}/6$ while achieving zero average CMV within one T_s period and zero mean CMV over a fundamental period. This effectively suppresses the 3rd and triple-order harmonic components in the CMV.

3.4 CMV Suppression Based on Three-Phase Four-Leg Topology

The topology of a three-phase four-leg inverter is shown in [Figure 10: see original paper]. The analysis principle is similar to that of the traditional three-leg topology. The CMV expression for the three-phase four-leg inverter is:

$$U_{no} = \frac{U_{1o} + U_{2o} + U_{3o} + U_{4o}}{4}$$

Since the numerator in this equation contains an even number of variables, the CMV can be suppressed to zero by adjusting different conduction states. For example, when the first three bridge legs are in state (100), the CMV is $-U_{dc}/6$.

This CMV can be compensated by controlling the conduction state of the fourth bridge leg to make U_{no} equal to zero. By enumerating the logic states of the four bridge legs, the control signal for the fourth bridge leg is determined to be $S_D = S_A \oplus S_B \oplus S_C$ (where the first three bridge legs are also controlled based on non-zero vector modulation). Thus, adding the fourth bridge leg can theoretically suppress the instantaneous CMV to zero.

4 Simulink Simulation Verification

The simulation parameters are: switching frequency of 1 kHz and modulation index of 0.8.

4.1 SVPWM Modulation Strategy

The simulation results are shown in [Figure 11: see original paper] and [Figure 12: see original paper].

4.2 AZSPWM Modulation Strategy

The simulation results are shown in [Figure 13: see original paper] and [Figure 14: see original paper].

4.3 NSPWM Modulation Strategy

The simulation results are shown in [Figure 15: see original paper] and [Figure 16: see original paper].

4.4 VSVM Modulation Strategy

The simulation results are shown in [Figure 17: see original paper] and [Figure 18: see original paper].

4.5 Three-Phase Four-Leg Control Strategy

The simulation results are shown in [Figure 19: see original paper].

5 Conclusion

Based on the simulation results, both AZSPWM and NSPWM schemes effectively suppress the CMV peak to $U_{dc}/6$, but the 3rd harmonic component in the CMV remains. The VSWM simulation results show that the 3rd and triple-order harmonic components are well suppressed, though the CMV peak remains at $U_{dc}/6$. Finally, by combining the non-zero vector modulation scheme with the three-phase four-leg inverter topology, the CMV is suppressed to nearly zero, demonstrating the best CMV suppression performance.

Compared with the AZSPWM, NSPWM, and VSVM schemes, the three-phase four-leg topology increases hardware cost. Moreover, the three-phase four-leg structure was originally proposed for handling three-phase unbalanced loads. The control scheme presented in this paper only utilizes 6 of the 16 available space voltage vectors and cannot support three-phase unbalanced loads, which means the full potential of this topology is not realized.

This paper provides a brief introduction and discussion of several common CMV suppression schemes through theoretical analysis and simulation verification, offering reference for research in CMV suppression.

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Note: Figure translations are in progress. See original paper for figures.

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