Power Line Carrier Communication for Servo Systems and Encoders: Postprint

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Abstract

For position precise control systems, a BISS-C protocol communication system based on DC power line carrier technology is proposed. The carrier communication system employs the BISS-C protocol, utilizes the DC power line as the transmission medium, and adopts asynchronous communication to achieve quasi-synchronous signal transmission, thereby simplifying the communication architecture, enhancing cable utilization efficiency, and enabling power supply and data communication multiplexing over a two-wire interface. With an FPGA as the core component, the system designs the carrier hardware circuitry, plans the communication procedures, and formulates the communication protocol. Servo motor closed-loop control experiments demonstrate that the system operates with stability and reliability, satisfying the communication requirements.

Full Text

Research on Communication Between Servo System and Encoder Based on Power Line Carrier Technology

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Abstract

For position-oriented precise control systems, this paper proposes a BISS-C protocol communication system based on DC power line carrier technology. The carrier communication system employs the BISS-C protocol and utilizes the DC power line as the transmission medium. By adopting asynchronous communication to achieve quasi-synchronous signal transmission, the system simplifies the communication architecture and improves cable utilization, enabling the multiplexing of power supply and data communication over just two wires. The

system employs a Field Programmable Gate Array (FPGA) as its core component, with designed carrier hardware circuits, planned communication flow, and established communication protocols. Experimental results from servo motor closed-loop control demonstrate that the system operates stably and reliably, meeting all communication requirements.

Keywords: Power line carrier, servo system, BISS-C protocol, FPGA

1 Introduction

High-performance servo drive systems typically employ high-resolution, high-speed encoders as position sensors for motors to obtain accurate position and velocity information [1]. Such encoders usually implement full-duplex synchronous serial communication to achieve high-speed, high-bit-rate, and highly reliable digital signal transmission that meets the demands of closed-loop servo drive control. Reducing the number of communication cables and interfaces represents a new paradigm for long-distance, high-reliability data transmission and bus architectures.

This paper utilizes power line carrier technology [2-3] to transform the full-duplex synchronous serial communication between servo motor rotary encoders and servo systems into half-duplex asynchronous communication, while still fulfilling the original full-duplex synchronous serial communication requirements between servo motors and servo systems, thereby achieving the goal of reducing signal lines and simplifying the communication system [4].

A DC carrier communication system based on the BISS-C protocol has been developed in this work. The BISS-C protocol is an open synchronous serial protocol with a communication baud rate of up to 10 Mbit/s, offering advantages such as openness and high speed, with leading capabilities in networking modes and delay compensation compared to other interfaces. It is primarily applied in motion control fields to enable communication between servo drives and encoders. Based on power line carrier communication technology and without altering the original BISS-C protocol communication method, this paper implements bidirectional communication using DC power lines.

The communication structure of the DC carrier communication system is shown in [Figure 1: see original paper]. The host and communication module 1, as well as the slave and communication module 2, still employ BISS-C-based full-duplex synchronous serial communication, while the two communication modules utilize half-duplex asynchronous serial communication between them.

2.1 BISS-C Networking Modes

The BISS-C protocol supports two networking modes: point-to-point mode and bus mode. In point-to-point mode, a master controller interface connects to only

one device containing multiple slave interfaces. The master controller interface provides clock signals to the slave interfaces through MA differential signal lines, while the slave interfaces transmit sensor data back to the master controller interface via SL differential signal lines, starting from the first slave interface. Bidirectional communication is possible between the master controller interface and slave interfaces. This structure is illustrated in [Figure 2: see original paper].

For bus configuration, all devices are connected in a daisy chain, with each device potentially containing multiple slave interfaces. The master' s MA line simultaneously provides clock pulses to all slaves. Each slave interface has two terminals (SLO and SLI), where the input of the next slave (SLI) links to the output of the previous slave (SLO). Each slave interface prioritizes transmitting its own data, then appends received data to the end of its transmission queue. The protocol imposes no limit on the number of connected slaves, with the structure shown in [Figure 2: see original paper].

2.2 BISS-C Frame Structure

[Figure 3: see original paper] shows the timing diagram for standard BISS-C Single Cycle Data (SCD) frame transmission. MA represents the synchronous clock generated by the master station, which transmits one inverted bit of master control data (CDM) at the end of transmission (during the BISS Timeout period). SLO carries the sensor data and one bit of slave control data (CDS) returned from the slave station, where CDS serves as a response to the CDM from the previous SCD frame. When control data transmission is unnecessary, CDM=0 and CDS=0.

Since each SCD frame allows the master to transmit only one CDM bit and the slave to return only one CDS bit, multiple SCD frames are required to complete the transmission and reception of a complete control command set.

3.1 Hardware Design

The communication modules are designed around Altera' s Cyclone IV EP4C6E FPGA, serving as the core chips for both communication module 1 and communication module 2. In communication module 1, the FPGA acts as a slave to the master controller, providing data read from the power line to the master controller. In communication module 2, the FPGA functions as a master to the sensor (typically an encoder), reading absolute position data from the photoelectric encoder using a point-to-point connection.

Since communication between the host and sensor employs RS-485 differential signaling before the rotary encoder is connected, the power line carrier communication modules (communication module 1 and communication module 2) must convert the FPGA' s output level signals to differential signals. This paper utilizes the SN65HVD78D level conversion chip from Texas Instruments.

Among all hardware designs, the coupling circuit is the most critical component, forming the core of ensuring reliable signal transmission [5]. This paper employs transformer coupling for signal coupling, as shown in [Figure 4: see original paper]. Given that this design is generally applied in servo control systems with high communication baud rates (typically 1–10 Mbit/s), transformer selection is crucial for achieving broadband signal coupling. Considering that communication module 2 will be integrated into the encoder in practical applications, where space is extremely limited, the transformer size must be minimized. This paper selects the PE-68386NL transformer from Pulse Electronics, featuring a 1:1 voltage ratio. Testing demonstrates reliable communication from 0.5 to 15 Mbit/s, meeting design requirements.

[Figure 4: see original paper] illustrates the overall coupling circuit structure, where the transformer serves as the coupling and decoupling component. The blocking inductor prevents high-frequency signals on the power line from being shorted by the DC power supply, while the DC-blocking capacitor isolates the power supply voltage. In the diagram, the blocking inductor is 100 H and the DC-blocking capacitor is 0.47 F.

3.2 Software Design

The program is developed in Verilog HDL under the Quartus II software compilation environment using a bottom-up modular approach. For communication module 1, the 底层 modules include an output module, sampling module, decoding module, encoding module, and command generation module, with the top-level module being a state machine responsible for initializing and functionally calling each 底层 module. For communication module 2, the 底层 modules include a reading module, sampling module, decoding module, encoding module, and command judgment module, with the top-level state machine module handling inter-module calls and initialization. The CLK clock for each 底层 module is provided by a Phase Locked Loop (PLL) through frequency division or multiplication. The workflow among modules is shown in [Figure 5: see original paper].

Differential Manchester encoding is adopted as the encoding scheme. The original data requires encoding because the raw signal may contain significant DC components, which are detrimental to transformer coupling. Differential Manchester code transitions at the middle of each code element, ensuring the encoded signal contains no DC component. The clock signal can be extracted from the encoded data for synchronization, and unlike Manchester code, differential Manchester encoding has no encoding ambiguity.

According to the BISS-C protocol standard, each transmission involves only one SCD frame, and both the data processing time (t_busy) and frame end 标志 time (BISS-Timeout) can be adjusted through delays and settings. Leveraging these characteristics, this paper proposes a parallel data reading and transmission scheme. For discussion convenience, communication module 1 and communica-

tion module 2 are denoted as CM1 and CM2, respectively. The clock signal between the master controller and communication module 1 is denoted as MA1, and the data signal as SL1. The clock signal between communication module 2 and the slave is denoted as MA2, and the data signal as SL2. The carrier signal between the two communication modules is PLC.

As shown in [Figure 5: see original paper], when the master controller reads data (i.e., when MA1 has clock pulses), CM1 pulls SL1 low at the second rising edge of MA1 to respond to the master controller. At this point, CM1 sends a data read command to CM2. Upon receiving this command, CM2 begins generating MA2 pulses and reading data from the encoder. Simultaneously while reading data, CM2 encodes and outputs the already-read data. After obtaining the data, CM1 begins decoding while transmitting the data to the master controller, and at the end of one data frame, reads the CDM bit level and forwards this level to the CM2 module.

CM2 sends the relayed CDM bit to the sensor, completing one full SCD frame transmission, and then waits for the next data transmission. When sending commands, the transmission begins with a 1-bit low-level start bit, followed by a 2-bit command word, and ends with a 1-bit high-level stop bit. Unlike data transmission, the baud rate after sensor data encoding is lower than that after command encoding, aiming to reduce the overall time required to complete an SCD frame. In practice, the differential Manchester encoding frequency on the PLC carrier cable matches the synchronous pulse frequency of MA2, meaning CM2' s data reading and transmission frequencies are identical and can share the same pulse signal.

[Figure 5: see original paper] shows the entire software' s ModelSim simulation waveform, illustrating the complete system workflow. MA1 represents pulses from the master controller, SLO1 represents data returned from communication module 1 (CM1) to the master controller, MA2 represents pulses from communication module 2 (CM2), and SLO2 represents sensor data (SCD frames) returned from the sensor. S1 and S2 are carrier signals, equivalent to the PLC mentioned above, representing encoded data signals and encoded command signals, respectively.

4 Experiments and Results Analysis

To verify the feasibility of this proposal, an experimental validation platform based on a servo system was built, as shown in [Figure 6: see original paper]. To evaluate the performance of the DC carrier communication system, the following experiments were conducted:

1. **Communication Bandwidth Experiment**: Results demonstrate reliable communication bandwidth between 500 Kbit/s and 10 Mbit/s.
2. **Communication Delay Verification Experiment**: At a baud rate of 1.25 Mbit/s, communication delay is within 3 s, meeting servo system precision requirements.

3. **Bit Error Rate Verification Experiment**: After 24 hours of continuous position reading from the servo motor, the measured bit error rate is less than 1E-9.
4. **Anti-Interference Experiment**: To test the DC communication system' s anti-interference performance, artificial interference was introduced to observe whether the system could quickly return to normal communication. The interference method involved connecting a 5 Ω resistor between the two DC power lines to create an artificial signal short. Results showed that when the interference was removed, the system immediately resumed normal communication 状态.

[Figure 7: see original paper] shows the communication waveform between CM1 module and the master controller, while [Figure 7: see original paper] illustrates the communication waveform between CM2 module and the sensor. Measurements indicate that compared with the original communication method, the power line carrier delay is approximately 3.2 s, which meets the precision requirements for servo systems under normal conditions. If needed, the communication baud rate can be further increased to reduce delay.

5 Conclusion

This paper investigated the interface characteristics and working principles of the BISS-C protocol. Based on the requirement for simplified communication systems, a DC power line carrier technology was designed and implemented for BISS-C protocol communication. A coupling circuit capable of meeting high-frequency communication requirements was designed according to DC channel characteristics, and a communication module structure with FPGA as the hardware core was developed. Based on detailed analysis of the BISS-C protocol, this paper proposed an FPGA-based parallel communication timing solution.

Experimental results demonstrate that this scheme fully guarantees the communication performance requirements under the BISS-C protocol.

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Note: Figure translations are in progress. See original paper for figures.