Postprint of SVPWM Algorithm Based on DC-Side Voltage Balance Control for Solid-State Transformers

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Date: 2018-06-15T00:00:00+00:00

Abstract

As a core device of the energy internet, the solid-state transformer (SST) provides voltage level conversion and isolation, effectively integrating distributed renewable energy sources. However, modular cascaded H-bridge SSTs suffer from voltage balancing issues among H-bridge modules. This paper first investigates the space vector pulse width modulation (SVPWM) and voltage balancing control principle for single-phase cascaded H-bridge SSTs with arbitrary numbers of cells. A control strategy is proposed wherein the SST's voltage loop regulates one H-bridge's DC-link voltage, while a new control loop incorporated into the SVPWM adjusts the vector pulse widths of the remaining H-bridges, thereby enabling the other H-bridge voltages to follow and achieving voltage equalization across all modules. Finally, simulation results validate the proposed control strategy.

Full Text

SVPWM Algorithm with DC-Side Voltage Balance Control for Solid-State Transformers

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DOI: 10.11985/2018.02.005

Abstract

As a core component of the energy internet, solid-state transformers (SSTs) provide voltage level conversion and electrical isolation, enabling effective integration of distributed renewable energy sources. However, modular cascaded

H-bridge SSTs suffer from voltage imbalance issues among individual H-bridge modules. This paper investigates the space vector pulse width modulation (SVPWM) technique and voltage balance control principles for single-phase cascaded H-bridge SSTs with arbitrary numbers of cells. A novel control strategy is proposed wherein the SST voltage loop regulates one H-bridge's DC bus voltage, while an additional control loop incorporated into the SVPWM modulates the vector pulse widths of the remaining H-bridges, forcing their voltages to track the master bridge and thereby achieving voltage balancing across all H-bridges. Simulation results verify the correctness and effectiveness of the proposed control strategy.

Keywords: Solid-state transformer, single-phase cascaded H-bridge, voltage balance

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1 Introduction

The energy internet has attracted widespread attention as a development direction for modern power grids to enhance power supply reliability and quality while integrating distributed renewable energy sources. References [**?**, **?**] introduced the concept of an "energy internet" based on solid-state transformers for distribution networks. Current research on SSTs primarily focuses on control strategies for three-stage topologies, which offer advantages in flexible energy control and functional implementability [**?**].

Cascaded H-bridge SSTs for AC/DC conversion employ multiple series-connected H-bridge modules, which reduces voltage and current stress on individual components [**?**]. However, structural asymmetries among cascaded units, component inconsistencies, varying delays, and power imbalances can cause DC bus voltage imbalances that affect normal operation of the SST and its control system [**?**]. Reference [**?**] proposed adding auxiliary voltage balancing circuits, which simplifies the control system but introduces complex topology, high cost, and increased losses. Reference [**?**] employed a 3D-SVPWM modulation strategy that achieves fast DC bus voltage balance without auxiliary circuits, while reference [**?**] utilized single-phase dq decoupling control to redistribute d-axis active power for DC-side voltage balancing, though both methods involve complex calculations. Reference [**?**] adopted single-phase SVPWM with a compensation component to adjust redundant basic vector durations for rapid DC bus voltage regulation, but was limited to SSTs with only two cascaded H-bridges.

This paper investigates SVPWM modulation and voltage balancing strategies for single-phase cascaded H-bridge SSTs. To address voltage and power imbal-

ance issues inherent in generic SVPWM methods for single-phase multi-H-bridge cascaded SSTs, a control strategy is proposed that regulates one H-bridge's DC bus voltage while adjusting the pulse widths of other H-bridges to achieve voltage tracking. Simulation results demonstrate the feasibility and correctness of the proposed approach.

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2 Solid-State Transformer Topology and Role in Energy Internet

2.1 Role of Solid-State Transformers in Energy Internet

As illustrated in [Figure 1: see original paper], solid-state transformers serve as crucial components in the energy internet, providing not only power conversion but also maintaining system compatibility and flexibility [**?**]. SSTs feature four ports: high-voltage AC grid, AC load, low-voltage DC load, and DC bus. By sharing information with various power sources and loads, SSTs coordinate energy flow among distributed energy resources, energy storage systems, loads, and the grid, effectively integrating distributed renewable energy and enabling efficient utilization of energy from both renewable systems and conventional generation.

2.2 Solid-State Transformer Topology

The SST topology is shown in [Figure 2: see original paper] [**?**]. The AC/DC stage employs multiple cascaded H-bridge modules, offering simple structure, strong scalability, and low control complexity. This approach effectively reduces switch stress while increasing the equivalent switching frequency, thereby lowering input current harmonics and reducing filter inductor volume [**?**]. The DC/DC isolation stage uses a phase-shifted full-bridge DC/DC converter (dual active bridge, DAB), which features simple structure, low switching losses, and convenient control. Phase-shifted pulses enable bidirectional power flow.

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3 SVPWM Algorithm for Single-Phase Cascaded H-Bridge Converters

The AC/DC stage utilizes a single-phase cascaded H-bridge converter. Each H-bridge can output three states: U_{dc}, 0, and $-U_{dc}$. Defining each H-bridge's states as:

$$S_i = \begin{cases} 1 & \text{if } S_{i1}, S_{i4} \text{ are on} \\ 0 & \text{if } S_{i2}, S_{i4} \text{ are on} \\ -1 & \text{if } S_{i2}, S_{i3} \text{ are on} \end{cases}$$

where $i = 1, 2, 3$. With three cascaded H-bridges, U_{ab} can output seven levels from $+3U_{dc}$ to $-3U_{dc}$. For n cascaded H-bridges, U_{ab} can output up to $2n + 1$ levels.

3.1 Sector Judgment and Vector Time Calculation

Sector judgment is illustrated in [Figure 4: see original paper], where U represents the modulation waveform. Let $U = V_m \sin(\omega t - \theta)$. The operating sector is determined based on the relationship between V_m and U_{dc}.

Within one switching period T, V_m is synthesized using the two nearest voltage levels of its sector. For example, when V_m is in Sector 2, it is synthesized by the large vector $V_{max} = 2U_{dc}$ and small vector $V_{min} = U_{dc}$. Based on the volt-second balance principle:

$$\begin{cases} V_{min}T_{min} + V_{max}T_{max} = V_{mT} \\ T_{min} + T_{max} = T \end{cases}$$

Solving these equations yields:

$$T_{min} = \frac{(V_{max} - V_m)T}{V_{max} - V_{min}}, \quad T_{max} = T - T_{min}$$

3.2 Vector State Sequence

Each voltage level vector (except $\pm 3U_{dc}$) has redundant states that produce the same U_{ab} but affect individual H-bridge DC capacitor voltages differently. To enhance SVPWM versatility for cascaded H-bridge multilevel converters and prevent level-skipping, this paper simplifies redundant vector selection: positive vectors consist of states 1 and 0, while negative vectors consist of states 0 and -1. To ensure equal charge/discharge time for each H-bridge's DC capacitor, all redundant vectors have equal duration. To avoid reverse-polarity pulses that generate reverse torque, each voltage vector transition involves switching of only one bridge leg. The vector state sequence for three cascaded H-bridges is shown in .

3.3 Capacitor Voltage Balance Control

Even with equal charge/discharge times, differences in H-bridge losses and system delays cause capacitor voltage imbalances. Capacitors are bypassed when switches S_{i1} and S_{i3} or S_{i2} and S_{i4} conduct. Current flow effects on capacitor voltage are shown in [Figure 5: see original paper]. When capacitor voltage and current share the same direction ($i_{V_h} \geq 0$), capacitor voltage increases; when opposite ($i_{V_h} \leq 0$), it decreases [**?**].

Analysis of the vector state sequence in reveals that vector U_{dc} appears in Sectors 2, 1, -1, and -2. For instance, when the converter operates in state 001, H-bridge 3's DC capacitor charges/discharges while H-bridges 1 and 2 are bypassed. In these sectors, states 001, 100, and 010 have equal durations. By detecting capacitor voltage and current directions to determine charge/discharge status, and maintaining the total duration of these three states constant, individual state durations can be adjusted to balance each H-bridge's DC capacitor voltage, as shown in [Figure 6: see original paper].

For example, when the modulation wave u is in Sector 2, state 001 duration increases by $d_{1T_{min}}/3$, state 010 duration increases by $d_{2T_{min}}/3$, and state 100 duration becomes $(1 - d_1 - d_2)T_{min}/3$ to maintain the total time. The constraints $-T_{min}/6 \leq d_1 \leq T_{min}/6$ and $-T_{min}/6 \leq d_2 \leq T_{min}/6$ prevent negative durations.

As the number of cascaded H-bridges increases, more control variables d_n ($n = 1, 2, ...$) are required, increasing control complexity. To better manage these variables and achieve capacitor voltage balance, a master-slave control strategy is proposed: one H-bridge's DC bus voltage is regulated as the master, while others follow. Using three cascaded H-bridges as an example, the first H-bridge serves as the master with its DC capacitor voltage controlled to the reference value $V_{dc1-ref}$, while the other H-bridges track this voltage to achieve balance. The control strategy is shown in [Figure 7: see original paper].

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4 Control Strategies

4.1 Cascaded H-Bridge Control Strategy

To achieve zero steady-state error control on the AC/DC side, this paper employs a single-phase dq transformation control strategy. Similar to three-phase dq transformation, this method converts AC quantities to DC through coordinate transformation, enabling zero steady-state error control using PI regulators, then converts back to AC to generate PWM waveforms. The control strategy is illustrated in [Figure 8: see original paper], which incorporates a virtual current lagging the actual current by 90°. The transformation matrices are:

$$T_{am/dq} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}, \quad T_{dq/am} = T_{am/dq}^{-1} = \begin{bmatrix} \sin\omega t & \cos\omega t \\ -\cos\omega t & \sin\omega t \end{bmatrix}$$

4.2 Phase-Shifted Full-Bridge DC/DC Converter Control Strategy

The phase-shifted full-bridge DC/DC converter uses phase-shifted PWM to enable bidirectional power flow. As shown in [Figure 9: see original paper], droop control provides the reference voltage U_{dc-ref}, which is then regulated by a voltage outer loop and current inner loop to maintain the DC bus voltage at the reference value.

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5 Simulation

To verify the proposed single-phase cascaded H-bridge voltage balancing SVPWM strategy and SST control strategy, simulations were conducted in MATLAB/Simulink using a three-H-bridge SST. Simulation parameters are listed in .

The grid-side voltage is shown in [Figure 10a: see original paper]. The AC/DC stage operates with seven levels using three H-bridge units. Grid voltage and current waveforms in [Figure 10b: see original paper] demonstrate unity power factor operation. [Figure 10c: see original paper] shows the grid-side current with low harmonics, minimizing SST impact on the grid.

[Figure 11: see original paper] presents SST AC/DC stage simulation waveforms. Initially, voltage balance control is disabled with equivalent resistances of 12Ω, 8Ω, and 16Ω connected to the three H-bridges, resulting in capacitor voltage imbalance. The first H-bridge DC bus voltage is maintained at 200V through single-phase dq transformation control. At 0.2s, capacitor voltage balance control is activated, causing the second and third H-bridge capacitor voltages to rapidly converge to the first bridge's voltage, achieving balance. Comparative analysis shows both the proposed strategy and the method in [**?**] achieve DC-side voltage balance quickly during imbalance, as demonstrated in [Figure 11: see original paper].

[Figure 12: see original paper] shows additional simulation results: [Figure 12a: see original paper] displays the phase-shifted PWM waveforms for the DAB converter enabling bidirectional power flow; [Figure 12b: see original paper] shows the DC bus port voltage; and [Figure 12c: see original paper] presents the low-voltage DC port voltage.

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6 Conclusion

As a core device in the energy internet, solid-state transformers play a vital role in energy coordination and conversion. This paper proposes a single-phase multi-H-bridge SVPWM method for the AC/DC stage of SSTs and addresses capacitor voltage imbalance in multi-H-bridge circuits through a master-slave control strategy. Simulation results validate the correctness and effectiveness of the proposed methods.

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Note: Figure translations are in progress. See original paper for figures.