Postprint: Implementation of Key Technologies for Satellite Dual-Mode Timing Devices

Authors: Cai Fan, Chen Li

Date: 2018-05-17T00:00:00+00:00

Abstract

By analyzing the shortcomings of Global Positioning System timing and the feasibility of BeiDou Satellite Navigation System timing, a design methodology for timing equipment that combines satellite dual-mode timing with multi-clock sources is proposed. The integrity monitoring algorithms and time-keeping algorithms involved in the timing equipment are studied, and a detailed analysis process is presented.

Full Text

Realization of Key Technologies for Dual-Mode Satellite Timing Equipment

Cai Fan[1], Chen Li[2]
[1]Nanjing Xiaozhuang University, Nanjing 211171
[2]Shanghai Astronomical Observatory, Chinese Academy of Sciences, Shanghai 200030

Abstract: By analyzing the limitations of Global Positioning System (GPS) timing and the feasibility of using the BeiDou Navigation Satellite System (BDS) for timing applications, this paper proposes a design methodology for dual-mode satellite timing equipment that integrates multiple clock sources. The research focuses on integrity monitoring algorithms and holdover algorithms employed in the timing device, providing a detailed analytical process for both.

Keywords: Global Positioning System; BeiDou Navigation Satellite System; satellite timing; integrity monitoring; holdover algorithm

Time serves as a fundamental physical quantity that plays a critical role not only in daily life and basic scientific research but also in national defense and economic development. High-precision time references, as one of the essential infrastructure platforms, can significantly enhance the stability of systems and

equipment. Satellite timing receivers and their applications represent an important project for addressing China's fundamental timing communication facilities, enhancing the reliability of time synchronization technology while promoting the adoption of the domestically developed BeiDou navigation system. Currently, GPS receivers dominate the Chinese market, whereas BDS users are primarily limited to government agencies and large enterprises. As the BeiDou system continues to evolve, its user base will expand considerably. Developing BeiDou/GPS dual-mode satellite timing receivers will help broaden the domestic market for China' s independently developed BeiDou system and reduce dependence on GPS [1].

The GPS system is a military-civilian dual-use system controlled by the U.S. military. Although currently available for global use, its long-term free availability to China is not guaranteed, posing significant security risks. Should the GPS satellite navigation system malfunction or be disabled by the U.S. during conflicts, the impact on China would be substantial. Presently, China' s satellite timing primarily relies on GPS, which suffers from single-source dependency, lack of autonomous control, poor short-term stability, and weak security [3]. The dual-mode satellite timing equipment employs multi-clock-source adaptive synchronization technology, with BDS, GPS, and external IRIG-B codes serving as mutual backup time synchronization sources. A high-stability oven-controlled crystal oscillator (OCXO) is utilized as the local clock to achieve high-precision holdover, ensuring the reliability and stability of the dual-mode synchronization system. Through GPS timing modules, BeiDou timing modules, and external IRIG-B code inputs, the device obtains standard Coordinated Universal Time (UTC) and pulse-per-second (PPS) signals, corrects the local crystal oscillator frequency, and generates various timing outputs that meet synchronization requirements [4].

This paper discusses the key technologies for dual-mode satellite timing, focusing on signal integrity detection, local holdover, PPS signal generation, and related technologies.

1 Overall Architecture

The hardware architecture of the dual-mode satellite timing device is illustrated in [Figure 1: see original paper]. The main components include a navigation module, holdover module, serial output module, NTP output module, PPS output module, B-code output module, power module, display/control module, and network management module. All internal modules communicate via a bus architecture, with signals transmitted through the motherboard. In the navigation module, the satellite OEM unit outputs time information and 1PPS signals to the holdover tracking unit within the holdover module. After locking onto the satellite signal, the local crystal oscillator in the holdover tracking unit outputs 1PPS and 10MHz signals to other modules within the device, while simultaneously generating various required output signals based on these timing references for transmission to relevant modules via the bus.

The serial output module, NTP output module, PPS output module, and B-code output module all handle external signal output, providing different time signal formats according to specific requirements. The display/control module manages the human-machine interface and timing application processing. The power module supplies DC power to all modules, while the network management module handles inter-module information scheduling and remote monitoring functions, with the capability to output relevant status information.

The holdover module hardware consists of a Field Programmable Gate Array (FPGA) and peripheral circuits, with holdover and timing algorithms running in both the FPGA and microcontroller. According to the overall software architecture, the program implementing these algorithms comprises a frequency division unit, signal generation unit, B-code (DC and AC) encoding unit, and serial communication unit. The signal generation unit contains three sub-units: signal integrity detection, holdover, and PPS generation. These units are connected in series within the software to function as an integrated program, requiring careful consideration of various factors such as navigation module status determination, necessitating a detailed design of the overall software operational architecture.

[Figure 2: see original paper] presents the overall software architecture diagram. The software operates according to the following sequence:

1. Upon device power-on, the integrity detection sub-unit and frequency division unit are activated. Navigation module health is determined by continuously comparing the intervals of three consecutive (or more) 1PPS signals. If the intervals are correct, the navigation module is deemed operational, a status flag is set, and the GPS 1PPS signal is used as the default external holdover reference. If abnormal, the system continues monitoring until proper operation is confirmed. The frequency division unit contains the clock generation program for the entire FPGA, utilizing a combination of the FPGA' s built-in phase-locked loop and counter-based division to generate all required clock signals.

2. Once the navigation module operates normally, the holdover sub-unit is activated. The satellite navigation chip' s 1PPS signal is fed into the holdover sub-unit to discipline the OCXO.

3. The PPS generation sub-unit produces the 1PPS signal required for subsequent B-code (DC and AC) encoding and serial communication units based on the holdover sub-unit' s output.

4. In the B-code (DC) encoding unit, an interrupt is triggered by the locally generated 1PPS signal to convert GPS or BeiDou navigation chip time information into B(DC) code. Similarly, the B-code (AC) encoding unit converts the time information into B(AC) code using interrupts triggered by the local 1PPS signal.

5. The serial communication unit outputs communication information, satel-

lite status, and time code data via serial interface.

This paper focuses on the integrity detection algorithm and holdover algorithm employed in these sub-units.

2 Signal Integrity Detection

The signal integrity detection sub-unit validates the navigation chip' s output signals to ensure the obtained 1PPS and time information are correct, stable, and valid. As shown in [Figure 2: see original paper], the integrity detection sub-unit serves as the prerequisite and foundation for the subsequent holdover sub-unit, PPS generation sub-unit, B-code encoding units, and serial communication unit.

The validation method involves continuously comparing the intervals of three consecutive 1PPS signals from the navigation chip. If correct, the chip is judged operational and a status flag is output; otherwise, monitoring continues until proper operation is confirmed. The device operates in three distinct timing states, with different external clock sources used for each state to ensure stability. The state switching process is as follows:

1. After power-on, both GPS and BeiDou navigation chips begin operation, with their 1PPS signals undergoing continuous detection.
2. If both GPS and BeiDou 1PPS signals pass validation, both modules are deemed operational, and the system enters Timing State 1, using GPS as the primary holdover reference and BeiDou as backup. If only the GPS 1PPS signal passes, the system enters Timing State 2 with GPS as the reference. If only the BeiDou signal passes, the system enters Timing State 3 with BeiDou as the reference.
3. In Timing State 1, GPS remains the reference even if an external satellite switching command is received, as long as both signals are present. If both GPS and BeiDou signals are lost simultaneously, the system transitions to internal holdover mode. If only BeiDou is lost, the system switches to Timing State 2, maintaining GPS as reference. If GPS is lost in this state, the system enters internal holdover; if BeiDou is reacquired, it returns to Timing State 1. If only GPS is lost, the system enters Timing State 3 using BeiDou as reference. If BeiDou is subsequently lost, internal holdover is initiated; if GPS is reacquired, the system returns to Timing State 1.
4. In Timing State 2, GPS serves as the holdover reference. Acquisition of BeiDou signals triggers a transition to Timing State 1, while loss of GPS signals initiates internal holdover.
5. In Timing State 3, BeiDou serves as the holdover reference. Acquisition of GPS signals triggers a transition to Timing State 1, while loss of BeiDou signals initiates internal holdover.

6. In internal holdover mode, simultaneous reception of both GPS and BeiDou 1PPS signals transitions the system to Timing State 1. Reception of only GPS signals transitions to Timing State 2, while reception of only BeiDou signals transitions to Timing State 3.

[Figure 3: see original paper] illustrates the timing state switching flowchart.

3 Holdover Technology

The primary hardware components of the holdover module in the dual-mode satellite timing device are shown in [Figure 4: see original paper]. The holdover module consists of a satellite navigation chip, clock processing chip, digital-to-analog converter (DA), and oven-controlled crystal oscillator (OCXO). The satellite navigation chip receives 1PPS signals and time information, while the clock processing chip feeds the 1PPS clock error to the microcontroller. This data is processed by the microcontroller to control the DA converter for OCXO correction, ensuring execution of the holdover sub-unit software.

The holdover sub-unit software operates by comparing the navigation chip' s 1PPS signal to generate a crystal oscillator 1PPS signal 80ms earlier. Every 128 seconds, the average clock error between the navigation chip' s 1PPS and the crystal oscillator' s 1PPS is sent to the microcontroller. After processing, the microcontroller controls the DA converter to adjust the OCXO, thereby completing the OCXO disciplining process to achieve high stability and accuracy.

The holdover sub-unit program comprises two parts: FPGA program and microcontroller program. The FPGA program includes clock processing and data communication components. The clock processing component measures the average clock error required for microcontroller-controlled DA conversion, accounting for navigation signal jitter, crystal aging drift, and oscillator inaccuracy. The microcontroller program primarily handles error control. The operational process is as follows:

1. The system receives 1PPS signals from both GPS and BeiDou navigation chips, generating two 80ms-advanced 1PPS signals (GPS-to-oscillator and BeiDou-to-oscillator) using a 100MHz reference clock.

2. Two sets of adjacent 128-second clock errors are continuously stored: one between the GPS 1PPS and the GPS-to-oscillator 1PPS, and another between the BeiDou 1PPS and the BeiDou-to-oscillator 1PPS. The average clock errors over 128 seconds are calculated for both GPS-to-local-oscillator and BeiDou-to-local-oscillator. In Timing States 1 and 2, the GPS-to-local-oscillator average error is sent to the microcontroller via serial interface according to the specified frame protocol. In Timing State 3, the BeiDou-to-local-oscillator average error is transmitted. In internal holdover mode, the previous GPS-to-local-oscillator average error is sent to the microcontroller.

3. The microcontroller adjusts the OCXO frequency via the DA converter

based on the error values from the FPGA, completing the OCXO disciplining process.

The algorithms discussed herein have been successfully implemented in dual-mode satellite timing equipment. The integrity detection algorithm ensures reliable operation across various satellite timing environments, while the holdover algorithm maintains long-term stability consistent with satellite timing. Multi-mode timing devices not only meet higher time synchronization requirements but also offer flexible configuration of inputs, outputs, and power supplies, with a rich selection of modules and cards. Both the types and quantities of timing signals can be flexibly configured, with multiple external timing systems providing mutual compatibility and backup. When one system fails, the receiver can rely on alternative systems to maintain normal operation, thereby improving overall equipment reliability and reducing dependence on single systems across various industries [5].

References

[1] 刑薇. 卫星授时接收机与测试系统的研究 [D]. 长沙：湖南大学，2011.
[2] 高新玉，张继宏，张远超. 北斗多模卫星导航在电力系统中同步授时研究 [J]. 电脑知识与技术，2014，10(16):3929-3932.
Gao Xinyu, Zhang Jihong, Zhang Yuanchao. Beidou satellite navigation and multi-mode timing synchronization in power system studies[J]. Computer Knowledge and Technology, 2014, 10(16):3929-3932.
[3] 陈孟元，凌有铸，王冠凌. 北斗卫星导航系统与 GPS 互备的广播电视授时单元 [J]. 电视技术，2010, 34(6):60-63.
Chen Mengyuan, Ling Youzhu, Wang Guanling. Broadcast television time service unit using mutually backup synchronization signals from Beidou satellite navigation and Global Positioning System[J]. Video Engineering, 2010, 34(6):60-63.
[4] 郭彬. 基于北斗 GPS 双模授时的电力系统时间同步技术研究 [D]. 长沙：湖南大学，2010.
[5] 聂建慧. 双模导航接收机精密授时系统的设计与实现 [D]. 北方工业大学，2014.

Note: Figure translations are in progress. See original paper for figures.