Establishment of the DBBC2 Digital Terminal System at the Nanshan Station of Xinjiang Astronomical Observatory (Postprint)

Authors: Yang Wenjun, Yang Jun, Jiang Wu, Xia Bo, Li Jian, Cui Lang, Zhang Hua, Li Peng, Gao Zhifu

Date: 2018-05-17T00:00:00+00:00

Abstract

With the rapid development of computer digital technology, the Base Band Converter (BBC), a key observation terminal device required for Very Long Baseline Interferometry (VLBI), has evolved from analog systems (Analog BBC, ABBC) to digital systems (Digital BBC, DBBC). Compared with analog systems, digital systems offer high flexibility and can exponentially increase VLBI observation bandwidth, thereby meeting various high-sensitivity VLBI observation requirements. Considering these technical advantages and the important role of the Nanshan Station of Xinjiang Astronomical Observatory in domestic and international VLBI networks, the station upgraded its VLBI terminal system in 2016, introducing a DBBC2 terminal developed by the Italian company Hat-Lab. This paper introduces the main components and working principles of the European DBBC2 system, as well as the methods for system assembly, connection, configuration, calibration, and debugging. After comprehensive inspection and testing of the system hardware and software, joint observations were conducted with major domestic and international stations, and correlated interference fringes were successfully obtained on multiple occasions. This series of successful observations demonstrates that the Nanshan DBBC2 system has been successfully installed and possesses high reliability. With the new DBBC2 system, Nanshan Station can participate in broadband VLBI observations with recording rates of 2/4 Gbps, which is extremely beneficial for astronomers to conduct mapping observations of fainter radio sources in the universe with milliarcsecond resolution.

Full Text

Installing a VLBI Digital Backend with DBBC2 at Nanshan Station, Xinjiang Astronomical Observatory

Yang Wenjun[1], , Yang Jun[2], Jiang Wu[3], Xia Bo[3], Li Jian[1], Cui Lang[1], Zhang Hua[1], Li Peng[1], Gao Zhifu[1]

[1] Xinjiang Astronomical Observatory, National Astronomical Observatories, Chinese Academy of Sciences, Urumqi 830011, China

[2] Onsala Space Observatory, Chalmers University of Technology, 43992 Onsala, Sweden

[3] Shanghai Astronomical Observatory, National Astronomical Observatories, Chinese Academy of Sciences, Shanghai 200030, China

Key Laboratory of Radio Astronomy, Chinese Academy of Sciences, Urumqi 830011, China

Abstract

With the rapid development of digital computer technology, the Base Band Converter (BBC)—a critical terminal device for Very Long Baseline Interferometry (VLBI) observations—has evolved from analog systems (Analog BBC, ABBC) to digital systems (Digital BBC, DBBC). Compared with analog systems, digital systems offer significantly greater flexibility and can substantially increase VLBI observation bandwidth, thereby meeting various high-sensitivity VLBI observation requirements. Considering these technical advantages and the important role of Nanshan Station in domestic and international VLBI networks, the station upgraded its VLBI terminal system in 2016 by introducing a DBBC2 terminal developed by Hat-Lab in Italy. This paper introduces the main components and working principles of the European DBBC2 system, as well as its assembly, connection, configuration, calibration, and debugging methods. After comprehensive testing of the system hardware and software, joint observations were conducted with major domestic and international stations, successfully obtaining correlation fringes on multiple occasions. These successful observations demonstrate that the Nanshan DBBC2 system has been successfully installed and exhibits high reliability. With the new DBBC2 system, Nanshan Station can participate in wideband VLBI observations with recording rates of 2/4 Gbps, which will greatly facilitate astronomers in mapping fainter radio sources with milliarcsecond resolution.

Keywords: DBBC2 System; VLBI; Base Band Converter

1. DBBC2 System Fundamentals and Composition

The DBBC2 system comprises several key modules including the CORE processing unit, connection server, FILA10G module, timing and clock board, and PC components. The intermediate frequency (IF) signal is fed to the analog signal conditioning module, where it undergoes filtering, shaping, and gain control before being sent to the AD sampler. After digitization, the signal travels via the High Speed Input (HSI) bus to the CORE data processing module for digital down-conversion and filtering into digital baseband signals. Finally, the data is output through the High Speed Output (HSO) bus and the VSI interface of the second FILA board. The VSI interface can connect to Mark5B data recording equipment or to the FILA10G module. A 1024 MHz frequency synthesizer generates the required sampling clock for the AD sampler. The PC component receives commands from the FS computer via the PCI bus to control the DBBC2, as illustrated in the schematic diagram [Figure 1: see original paper].

2. DBBC2 Structure

The DBBC2 system is housed in a chassis measuring 483 mm wide, 370 mm high, and 500 mm deep. On the lower portion of the front panel, blue indicator lights signify that the main power switch is active, as shown in [Figure 2: see original paper]. The rear panel features multiple connectors and interfaces, including three switches in the lower left corner—one large and two small. The large switch serves as the main power connection, while among the two smaller power switches, the red button controls power to the electronic components and the green button controls power to the internal PC system. The power-on sequence proceeds from left to right, with the power-off sequence being the reverse, as depicted in [Figure 3: see original paper].

The internal structure of DBBC2 primarily consists of four major sections: the electronic components, PC system, cooling system, and power supply system, as shown in [Figure 4: see original paper].

3. DBBC2 Main Performance Specifications

The main performance specifications of DBBC2 are summarized in . The system features selectable IF filter outputs covering 1-512 MHz, 512-1024 MHz, 1024-1536 MHz, and 1536-2058 MHz. Channel bandwidth options include 32, 16, 8, 4, 2, and 1 MHz for the V105E version. The AD sampler operates with a 1024 MHz sampling clock, while the CORE2 processing module supports Mark5B formatting, 10G fiber output, and VSI input/output. The system is controlled via FILA boards running on a Windows XP platform with PCI 7200 and PCI9111HR interfaces, plus JTAG connectivity.

4. DBBC2 Software and Observation Modes

The DBBC2 software operates in a Windows XP environment. The control software resides in the `c:\DBBC\bin` directory, user manuals are located in `c:\DBBC\doc`, configuration files are stored in `c:\DBBC_CONF\`, and firmware files are kept in `c:\DBBC_CONF\FilesDBBC`. The primary software applications include `DBBC2 Control DDC V105_1.exe` and `DBBC2 Control DDC`

`V105E_1.exe`. The system supports two main observation modes: DDC and PFB. The DDC mode is tunable with channel bandwidth ranging from 1-16 MHz, supports both upper and lower sidebands, and provides continuous 80 Hz synchronous calibration. Available observation modes include geo, astro, astro2, W-astro, VLBA, and test. The DDC mode also includes DDC-E, which extends bandwidth to 32 MHz for astro3 observation mode. The PFB mode employs fixed tuning with channel bandwidths of 32/64 MHz, using either upper or lower sideband depending on Nyquist sampling considerations.

5. System Installation and Testing

5.1 Hardware Connection and Self-Test

The installation procedure involves several critical steps. First, connect the 10 MHz reference signal (approximately 0 dBm amplitude) and 1 pps signal to the rear panel of DBBC2, then connect the VSI output cable from DBBC2 to the Mark5B recorder. After applying 220V power and configuring the IP address to integrate DBBC2 into the VLBI terminal network, the power-on sequence begins with the main power switch on the rear panel lower left, followed by the industrial computer power and finally the PC power. Upon launching the DDC software from the Windows XP desktop, the system configures the hardware, programming the four FPGA chips within DBBC2 with local oscillator frequencies. After programming completes, all board LEDs display identical patterns. The four columns of lights on the front panel flash sequentially before synchronizing at a 1 Hz frequency, indicating normal system operation. Configuration files must be edited according to the manual to select different IF inputs for ADB and adjust signal amplitude via AGC. The `DBBC client v4.exe` program allows testing of IF power levels, bandwidth, and attenuation by entering commands at the "Enter Command:" prompt. Mark5B must synchronize to the 1 pps signal transmitted through the VSI cable by running the `tstDIM` program and executing time synchronization commands as detailed in the Mark5B manual.

5.2 Clock Calibration

Clock calibration utilizes a 764 MHz signal at approximately -15 dBm amplitude, split through a 1:4 power divider to feed DBBC2 rear panel inputs IFA1, IFB1, IFC1, and IFD1. The internal IF filter output is set to filter #2 (512-1024 MHz) for all channels. Detailed calibration procedures are available in the referenced documentation.

5.3 FS-Related Settings

Three key configuration steps are required for Field System (FS) integration. First, modify the `dbbad.ctl` file in the `/usr2/control/` directory on the FS computer to include DBBC2' s IP address using port 4000. Second, for clock difference collection during observations, modify the `ibad.ctl` file to define port

C2 as `C2=dev03,0`, then run the `clock` command in the FS operator window to verify proper reading of clock differences. Third, point noise control—used to test system temperature by controlling the receiver noise source—requires setting the serial port in the `stqkr.c` file located in `/usr2/st/stqkr/` with the format `pcaltty_numb="/dev/ttyr03"`. After recompiling, test communication using `cal=on` and `cal=off` commands in the FS operator window. Finally, update the `equip.ctl` file to specify rack type as `dbbc`, version as `v105_1`, Mark5B clock rate as 32, and FiLa10G input as `vsi1`.

6. Testing Results and Performance Verification

On January 12, 2017, Nanshan Station conducted S/X-band fringe tests in conjunction with Kunming Station and Shanghai Tianma Station, successfully obtaining interference fringes. On February 23 and 25, Nanshan Station performed L-band fringe tests with European EVN stations, again successfully acquiring fringes. On March 21, Nanshan Station participated in EVN gr039 observations, simultaneously recording with both DBBC2 and ABBC equipment. Post-experiment analysis involved cross-correlating data from the same time periods with Shanghai Tianma Station. The processing results [Figure 5: see original paper] clearly demonstrate superior performance from DBBC2 [FIGURE:5(a)] compared to ABBC [FIGURE:5(b)]. On April 3, Nanshan Station and Tianma Station conducted K-band fringe detection experiments, achieving excellent results as shown in [Figure 6: see original paper]. These domestic and international joint tests confirm the successful establishment of the Nanshan DBBC2 system.

6.1 Challenges During Upgrade

Several technical issues were encountered during the upgrade process. First, the DBBC2 rear panel lacks a dedicated VSI connector, requiring custom fixation for internal VSI cables. Second, upon delivery, the connection plugs and sockets between FILAIN, ADB1/2, CORE, and FILAOUT circuit boards were disconnected. After reconnecting all interfaces and powering the system, software loading failed with no clear diagnostic from indicator lights. Analysis revealed that insufficiently tight connections between board connectors prevented proper software loading; firm reseating resolved the issue. Third, initial tests showed low signal-to-noise ratios in correlated data, initially attributed to insufficient input signal amplitude. However, increasing input amplitude did not improve results. Through systematic analysis, the solution required *reducing* input signal amplitude, as the internal signal was approaching saturation—a key difference between DBBC2 and both ABBC and CDAS (Chinese Data Acquisition System) regarding optimal input levels.

6.2 IF Wiring Configuration for Operations

Once all DBBC2 tests are completed, the system is ready for formal domestic and international joint observations. However, the observation planning team requires the station' s IF connection diagram showing how receiver signals from various bands are allocated to DBBC2 inputs. This information enables them to design appropriate observation modes and BBC channel allocations. [Figure 7: see original paper] presents the DBBC2 IF wiring diagram for Nanshan Station.

7. Conclusion

Driven by advances in very-large-scale integration and software-defined radio technology, digital baseband converters (DBBC) have gradually replaced analog recording terminals (ABBC) worldwide. Compared with analog equipment, DBBC offers superior cost-effectiveness, better passband characteristics, and improved stability and reliability metrics. Comprehensive testing of the DBBC2 system at Nanshan Station confirms that all technical specifications meet requirements. Joint test results with domestic and international stations demonstrate performance superior to the original analog baseband converter, while operational procedures are significantly more convenient. The successful implementation of the Nanshan DBBC2 system marks the definitive end of the global VLBI analog baseband converter era. The new system will undoubtedly play a crucial role in future VLBI observations.

Acknowledgments

We thank Kunming Station of Yunnan Astronomical Observatory and Shanghai Tianma Station for their support during Nanshan DBBC2 fringe tests. We also acknowledge assistance from Shanghai Astronomical Observatory engineers Zhao Rongbing and Jiang Yongbin, and Xinjiang Astronomical Observatory engineers Li Guanghui, Chen Yong, Liu Feng, and Li Xiaofei for their help with software control and hardware testing.

References

[1] Yang Wenjun, Hao Longfei. Development history and future prospects of VLBI terminals [J]. Astronomical Research & Technology-Publications of National Astronomical Observatories of China, 2012, 9(4): 374-381.

[2] Zhang Bijuan, Wu Yajun, Yu Wei, et al. A method of calculating the quantization threshold for a VLBI DBBC and its FPGA implementation[J]. Astronomical Research & Technology-Publications of National Astronomical Observatories of China, 2013, 10(3): 219-226.

[3] Zhu Renjie, Zhang Xiuzhong, Wei Wenren, et al. The progress of modern Chinese data acquisition system[J]. Progress in Astronomy, 2011, 29(2): 207-217.

[4] Wu Yajun, Liu Qinghui, Li Juan, et al. Spectral line observation and data calibration of Tianma 65m radio telescope [J]. Astronomical Research & Technology, 2017, 14(1): 1-7.

[5] Xiang Binbin, Liu Zhiyong, Yang Wenjun. Antenna measurement of Urumqi VLBI radio telescope with field system [J]. Astronomical Research & Technology–Publications of National Astronomical Observatories of China, 2014, 11(4): 343-349.

[6] Hong Xiaoyu, Cao Ning. VLBI Digital Base Band Convert [J]. Bulletin of Chinese Academy of Sciences, 2011, 26(5): 593-596.

Note: Figure translations are in progress. See original paper for figures.