Postprint of Key Technology Implementation for Satellite Dual-Mode Timing Device

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Abstract

By analyzing the shortcomings of Global Positioning System (GPS) timing and the feasibility of BeiDou Satellite Navigation System for timing, a design methodology for a timing device combining satellite dual-mode timing with multi-clock sources is proposed. The integrity monitoring algorithms and time-keeping algorithms involved in the timing device are investigated, and a detailed analysis process is presented.

Full Text

Realization of Key Technologies in Dual-Mode Satellite Timing Equipment

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Abstract: By analyzing the limitations of GPS timing and the feasibility of BeiDou satellite navigation system for timing applications, this paper proposes a design methodology for dual-mode satellite timing equipment integrated with multi-clock sources. The research focuses on integrity monitoring algorithms and timing-hold algorithms employed in the equipment, providing a detailed analytical process for both.

Keywords: GPS; BeiDou Navigation Satellite System; satellite timing; integrity monitoring; timing-hold algorithm

Time, as a fundamental physical quantity, plays a crucial role not only in daily life and basic scientific research but also in national defense and economic development. High-precision time references, as one of the essential infrastructure platforms, can significantly enhance the stability of systems and equipment.

Satellite timing receivers and their applications represent an important project for addressing fundamental timing communication infrastructure in China, enhancing the reliability of time synchronization technology while promoting the adoption of the domestically developed BeiDou Navigation Satellite System. Currently, GPS receivers dominate the Chinese market, whereas BeiDou system users are primarily limited to government agencies and large enterprises. As the BeiDou system continues to evolve, its user base will expand considerably. Developing dual-mode GPS/BeiDou satellite timing receivers will help broaden the domestic market for China' s independently developed BeiDou system and reduce dependence on GPS. The GPS system, controlled by the U.S. military and available for both military and civilian use, remains accessible worldwide but without any guarantee of indefinite free usage for China, posing significant security risks. Should the GPS satellite navigation system malfunction or be altered or shut down by the U.S. during conflicts, the impact on China would be substantial.

At present, China' s satellite timing primarily relies on GPS, which suffers from single-source dependency and lack of autonomous control, resulting in poor short-term stability and weak security. Dual-mode satellite timing equipment employs multi-clock source adaptive synchronization technology, with BeiDou, GPS, and external IRIG-B code serving as mutually compatible time synchronization systems for the device. A high-stability oven-controlled crystal oscillator (OCXO) is utilized as the local clock to achieve high-precision timing-hold, ensuring the reliability and stability of the dual-mode synchronization system. Through GPS timing modules, BeiDou timing modules, and externally input IRIG-B code, standard UTC time information and 1PPS signals are obtained to correct the local crystal oscillator frequency, generating various timing outputs that meet synchronization requirements. This paper discusses the key technologies for dual-mode satellite timing, focusing on signal integrity detection, local timing-hold, and 1PPS signal generation.

1 Overall Architecture

The hardware architecture of the dual-mode satellite timing receiver is illustrated in [Figure 1: see original paper]. The system primarily comprises navigation modules, a timing-hold module, serial output module, NTP output module, 1PPS output module, B-code output module, power supply module, display/control module, and network management module. Internal communication between modules employs a bus architecture, with signals transmitted through the motherboard. In the navigation module, the satellite OEM unit outputs time information and 1PPS signals to the timing-hold tracking unit within the timing-hold module. After locking onto satellite signals, the local crystal oscillator in the timing-hold tracking unit outputs 1PPS and 10MHz signals to other modules within the receiver. Simultaneously, based on these 1PPS and 10MHz signals, various required output signals are generated and transmitted via the bus to relevant modules.

The serial output module, NTP output module, 1PPS output module, and B-code output module all handle external signal output, providing different time signal formats or information according to specific requirements. The display/control module manages human-machine interface operations and timing application processing. The power supply module provides DC power to all modules, while the network management module handles inter-module information scheduling and remote monitoring functions, with the capability to output relevant status information.

The timing-hold module hardware consists of a Field Programmable Gate Array (FPGA) and peripheral circuits, with timing and timing-hold algorithms running in the FPGA and microcontroller—constituting the device' s software program. Based on the overall algorithm architecture, the software is partitioned into a frequency division unit, signal generation unit, B-code (DC and AC) encoding unit, and serial communication unit. The signal generation unit contains three sub-units: signal integrity detection, timing-hold, and 1PPS generation sub-units. In the software program, these units are connected in series to form an integrated operational program, requiring careful consideration of various factors such as navigation module status determination. Consequently, the overall software architecture must be meticulously designed. [Figure 2: see original paper] presents the overall software block diagram.

The software program operates according to the following sequence: (1) Upon power-on, the signal integrity detection sub-unit and frequency division unit are activated. The navigation module' s operational status is determined by continuously comparing the intervals of three consecutive 1PPS signals (though more samples may be used). If the intervals are correct, the navigation module is deemed operational, a flag is set, and GPS 1PPS signals are used as the default external timing reference. If incorrect, the navigation module continues to be monitored until normal operation is confirmed. The frequency division unit contains the clock generation program for the entire FPGA, utilizing a combination of the FPGA' s built-in phase-locked loops and counter-based division to generate all required clock signals. (2) Once the navigation module operates normally, the timing-hold sub-unit is activated. The satellite navigation chip' s 1PPS signal is fed into the timing-hold sub-unit to discipline the OCXO. (3) The 1PPS generation sub-unit then produces the 1PPS signals required for subsequent B-code (DC and AC) encoding and serial communication units based on the timing-hold sub-unit' s output. (4) In the B-code (DC) encoding unit, an interrupt is triggered by the locally generated 1PPS signal to convert GPS or BeiDou navigation chip time information into B(DC) code. Similarly, in the B-code (AC) encoding unit, an interrupt triggered by the locally generated 1PPS signal converts the navigation chip time information into B(AC) code. (5) The serial communication unit outputs communication information, satellite status, and time code information via the serial port.

This paper focuses on the signal integrity detection algorithm and timing-hold algorithm employed in these sub-units.

2 Signal Integrity Detection

The signal integrity detection sub-unit validates the navigation chip's output signals to ensure the obtained 1PPS and time information are correct, stable, and valid. As shown in [Figure 2: see original paper], the signal integrity detection sub-unit serves as the prerequisite and guarantee for the subsequent operation of the timing-hold sub-unit, 1PPS generation sub-unit, B-code (DC and AC) encoding units, and serial communication unit.

The validation method involves continuously comparing the intervals of three consecutive 1PPS signals from the navigation chip. If the intervals are correct, the navigation chip is judged to be operating normally and a status flag is output. If incorrect, the navigation chip continues to be monitored until normal operation is confirmed. The equipment operates in three distinct timing-hold states, with different external clock sources employed for each state to ensure timing stability. The state transition flow is illustrated in [Figure 3: see original paper].

The operational flow proceeds as follows: (1) After power-on, the GPS and BeiDou navigation chips begin operation, and their respective 1PPS signals undergo continuous monitoring. (2) If both GPS and BeiDou 1PPS signals pass validation, both navigation modules are deemed operational, and the system enters Timing-Hold State 1, using GPS signals as the primary timing reference while BeiDou signals serve as backup. If only the GPS 1PPS signal passes validation, the GPS chip is judged operational while the BeiDou chip is not, prompting entry into Timing-Hold State 2 with GPS as the timing reference. If only the BeiDou 1PPS signal passes validation, the BeiDou chip is judged operational while GPS is not, resulting in Timing-Hold State 3 with BeiDou as the timing reference. (3) While in Timing-Hold State 1, if both GPS and BeiDou signals remain available, GPS continues as the timing reference even upon receiving external satellite switching commands. If both satellite signals are lost simultaneously, the system transitions to internal timing-hold mode. If only BeiDou signals are lost, the system enters Timing-Hold State 2, maintaining GPS as the reference. If GPS signals are lost in this state, the system transitions to internal timing-hold; if BeiDou signals are reacquired, the system returns to Timing-Hold State 1. If only GPS signals are lost, the system enters Timing-Hold State 3, using BeiDou as the reference. If BeiDou signals are subsequently lost, the system enters internal timing-hold; if GPS signals are reacquired, the system returns to Timing-Hold State 1. (4) In Timing-Hold State 2, GPS serves as the timing reference. If BeiDou signals are acquired, the system transitions to Timing-Hold State 1; if GPS signals are lost, it enters internal timing-hold mode. (5) In Timing-Hold State 3, BeiDou serves as the timing reference. If GPS signals are acquired, the system transitions to Timing-Hold State 1; if BeiDou signals are lost, it enters internal timing-hold mode. (6) In internal timing-hold mode, if both GPS and BeiDou 1PPS signals are received, the system transitions to Timing-Hold State 1; if only GPS 1PPS is received, it enters Timing-Hold State 2; if only BeiDou 1PPS is received, it enters Timing-Hold State 3.

3 Timing-Hold Technology

The primary hardware components of the timing-hold module in the dual-mode satellite timing receiver are shown in [Figure 4: see original paper]. The timing-hold module consists mainly of a satellite navigation chip, clock processing chip, digital-to-analog converter (DAC), and oven-controlled crystal oscillator (OCXO). The satellite navigation chip receives 1PPS signals and time information from the navigation satellites, while the clock processing chip feeds the 1PPS clock error to the microcontroller. This data is processed by the microcontroller to control the DAC, which corrects the OCXO. The timing-hold module ensures the execution of the timing-hold sub-unit software.

The timing-hold sub-unit software operates by comparing the locally generated 1PPS signal with the navigation chip' s 1PPS signal, producing a crystal-derived 1PPS signal that leads the reference by 80ms. Every 128 seconds, the average clock error between the navigation chip' s 1PPS and the crystal-derived 1PPS is sent to the microcontroller, which processes this data to control the DAC for OCXO correction, thereby disciplining the OCXO to achieve high stability and accuracy.

The entire timing-hold sub-unit program is divided into FPGA and microcontroller components. The FPGA program primarily includes clock processing and data communication sections. The clock processing section measures the average clock error required for microcontroller DAC control, accounting for errors from navigation signal jitter, crystal aging drift, and oscillator inaccuracy. The microcontroller program mainly comprises error control logic. The operational sequence is as follows: (1) The system receives 1PPS signals from both GPS and BeiDou navigation chips, generating two 80ms-advanced 1PPS signals—one referenced to GPS and one to BeiDou—using a 100MHz base clock. (2) Two sets of adjacent 128-second clock errors are continuously stored: the error between the GPS 1PPS and the GPS-referenced crystal 1PPS, and the error between the BeiDou 1PPS and the BeiDou-referenced crystal 1PPS. The average clock errors between GPS time and the local oscillator, and between BeiDou time and the local oscillator, are calculated over the 128-second intervals. In Timing-Hold States 1 and 2, the GPS-local oscillator average error is transmitted to the microcontroller via serial port according to the specified frame protocol. In Timing-Hold State 3, the BeiDou-local oscillator average error is transmitted. In internal timing-hold mode, the previous GPS-local oscillator average error is sent to the microcontroller. (3) The microcontroller uses the error values from the FPGA to output control voltage through the DAC, adjusting the OCXO frequency to complete the disciplining process.

4 Conclusion

The processing algorithms described herein have been successfully implemented in dual-mode satellite timing equipment. The integrity detection algorithm ensures reliable operation across diverse satellite timing environments, while

the timing-hold algorithm maintains long-term stability consistent with satellite timing performance. Multi-mode timing equipment not only meets higher time synchronization requirements but also offers flexible configuration of inputs, outputs, and power supplies, with a rich selection of modules and cards available. The types and quantities of timing signals can be flexibly configured as needed, with multiple external timing systems providing mutual compatibility and backup. When one system fails, the receiver can continue normal operation using alternative systems, thereby enhancing overall equipment reliability and reducing the current over-reliance on single systems across various industries.

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Note: Figure translations are in progress. See original paper for figures.