Design and Implementation of a Digital Terminal for Low-Frequency Radio Antennas (Postprint)

Authors: Zhang Jinpeng, He Lesheng, Dong Liang, Wang Ting, Xuemin Li

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Abstract

Since astronomical observations entered the era of all-band observation, low-frequency radio signals in the full band have emerged as a new important observational band and research window. As information in this band is of great significance for studying radio bursts from the Sun and planets, and research on this frequency band remains largely unexplored, several European and American countries as well as our nation have timely initiated relevant research. At present, the Yunnan Astronomical Observatory of the Chinese Academy of Sciences has commenced construction of this project, with four low-frequency radio antennas now available for testing and use. Its low-frequency radio antenna array can be used in conjunction with the existing lOm solar radio telescope and 11 m solar radio telescope at the Yunnan Astronomical Observatory to observe radio information from the Sun or other planets with greater precision. The design first involves the A/D board receiving low-frequency astronomical signals from the low-frequency radio antennas; the A/D board then transmits the converted digital signals in differential form to the Field Programmable Gate Array (FPGA) board; the FPGA integrates and processes the data, transmitting it via Gigabit Ethernet using the UDP protocol through asynchronous First Input First Output (FIFO) across clock domains to the PC end; subsequently, software designed on the PC end performs windowing and Fast Fourier Transform processing on the transmitted data and displays it.

Full Text

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Zhang Jinping[1], He Lesheng[2], Dong Liang[2], Wang Ting[1], Li Xuemin

[1]School of Information Science and Engineering, Yunnan University, Kunming, Yunnan

[2]Yunnan Observatories, Chinese Academy of Sciences, Kunming, Yunnan
[3]Key Laboratory for the Structure and Evolution of Celestial Objects, Chinese Academy of Sciences, Kunming, Yunnan
Kunming Medical University Haiyuan College, Kunming, Yunnan

Abstract

Since astronomical observation entered the era of full-waveband observation, low-frequency radio signals have emerged as a new and important observational band and research window. Information in this band is crucial for studying radio bursts from the Sun and other planets, yet research in this frequency range remains largely unexplored. Consequently, several European and American countries, along with China, have initiated relevant research programs. The Yunnan Observatories of the Chinese Academy of Sciences has launched a construction project for this purpose, with four low-frequency radio antennas currently available for testing. The low-frequency radio antenna array can be used in conjunction with the existing ten-meter and eleven-meter solar radio telescopes at Yunnan Observatories to more accurately observe radio information from the Sun and other planets. In this design, an A/D converter card first receives low-frequency astronomical signals from the antenna and transmits the converted digital signals as differential signals to a Field-Programmable Gate Array (FPGA) card. The FPGA integrates and processes the data, then transfers it across clock domains using an asynchronous First-In-First-Out (FIFO) buffer to a PC terminal via Gigabit Ethernet using the User Datagram Protocol (UDP). Finally, software on the PC terminal performs windowing and Fast Fourier Transform (FFT) processing on the transmitted data for display.

Keywords: low-frequency radio antennas; FPGA; asynchronous FIFO; UDP; Gigabit Ethernet

Background and Research Significance

Astronomical observation serves as one of the most important methods for exploring the mysteries of the universe, with its research directions and scope continuously expanding. Modern astronomy has entered the era of full-waveband observation, and low-frequency radio waves (10–250 MHz) represent a new key observational and research window. This frequency band' s radio radiation is significant for studying solar and planetary radio bursts. Below 80 MHz, the very high frequency (VHF) band provides substantial information about solar and planetary radio emissions. This frequency range is not merely a simple extrapolation of currently observable electromagnetic wavebands but holds major significance and importance, as it has rarely been observed with effective spatial resolution. Human understanding of this frequency range is almost nonexistent, and many astronomical phenomena can only be detected in the very low-frequency band, making research in this area particularly important. Scientific detection content includes solar coronal mass ejections, radio bursts, Jovian radio emissions, low-frequency and very low-frequency pulsar radiation,

and hydrogen distribution detection. Due to the unknown nature of this band, there is also great potential for discovering entirely new phenomena.

In response to its practical significance and the urgent need to develop low-frequency capabilities, the Yunnan Observatories of the Chinese Academy of Sciences is constructing a low-frequency radio astronomy platform suitable for multiple scientific objectives, with an operating frequency range of 70–700 MHz (and 30–80 MHz for solar observations). This platform can work in conjunction with existing solar radio telescopes (625–1500 MHz) to achieve spectral observations. China's radio astronomy has made significant progress from meter-wave to millimeter-wave bands, implementing meter-wave synthetic aperture arrays and very long baseline interferometry at centimeter wavelengths, while participating in international projects such as the Atacama Large Millimeter/submillimeter Array and Antarctic terahertz astronomical observation programs. In recent years, China has also made substantial advances in technologies such as receiving area radio arrays and fixed-direction low-frequency cosmic radio arrays. However, in the decameter-wave measurement domain (60–230 MHz), only a few countries' observatories are conducting very low-frequency astronomical observations, making the development of China' s ground-based low-frequency radio observation research highly significant [1].

System Design Model

The system design model is shown in [Figure 1: see original paper]. The process begins with receiving two analog signals from the low-frequency radio antenna. An analog-to-digital converter transforms these into two 14-bit digital signals. The FPGA processes the acquired data and performs FFT processing before transmission. Data is then sent via Gigabit Ethernet using UDP. Finally, PC terminal software receives the data, integrates and processes it, achieving the design of the observation terminal [2]. The system includes both manual triggering and automatic triggering mechanisms.

This paper focuses on the FPGA data processing component and the PC data integration and processing component in the digital observation terminal design, primarily including asynchronous cross-clock-domain data processing, Gigabit Ethernet transmission, and PC-side data sorting and FFT processing. The detailed data processing flow is shown in [Figure 2: see original paper].

FPGA Hardware Design

2.1.1 Asynchronous FIFO Cross-Clock-Domain Processing

For asynchronous processing, signals from the ADC card first undergo differential-to-single-ended conversion, followed by simplified metastable circuit processing. Both channels of data are 14-bit, but the Gigabit Ethernet transmission format uses a minimum unit of 8-bit bytes. Therefore, the two channels of data must be integrated. The data reading width is 64 bits. This

project combines channels A and B into a new 64-bit data word, with channel A data in the high bits and channel B data in the low bits. Because the Gigabit Ethernet transmission unit requires byte alignment, a zero is padded to the most significant bit, resulting in the required 64-bit data. The data depth is determined by each data transmission volume.

When configuring FIFO parameters, independent read and write clocks are selected. The write clock is the system master clock at 245.76 MHz, while the read clock is the Gigabit Ethernet clock at 125 MHz. Due to the different clock domains, read and write signals must be controlled to prevent overflow. Given the enormous data volume, complete processing is impossible, so segmented caching and transmission are employed. Each segment is 0.5 MB, which is also the project' s maximum usable depth [3].

The asynchronous FIFO buffer sequential logic is controlled by a state machine. The initial state has both read and write flags at 0. When an external trigger key is pressed, the write flag becomes 1 and data writing begins. At this point, the empty flag is 0 and the full flag is 0, while the read flag remains 0. When 131,072 data words have been written, the write flag becomes 0, the full flag becomes 1, and the read flag becomes 1, starting data reading until all data is read. Signals are then fed back to the read and write flags, the read flag becomes 0, the write flag becomes 0, the empty flag becomes 1, and the full flag becomes 0, returning to the initial state. This completes one full cross-clock-domain read-write cycle. The next external trigger or timed automatic trigger begins a new cycle. The specific flow is shown in [Figure 3: see original paper].

2.1.2 Gigabit Ethernet Design and Implementation

The design employs an integrated Gigabit Ethernet MAC core. The transmission logic is implemented through control signals including `tx_axis_mac_tlast`, `tx_axis_mac_tready`, `tx_axis_mac_tuser`, and `tx_axis_mac_tvalid` [4-5]. The design simplifies the original timing and redefines transmission intervals according to actual requirements [6]. The Gigabit Ethernet MAC core model is shown in [Figure 4: see original paper].

After processing network card address information and meeting trigger conditions, frame header information must first be transmitted. The frame header consists of 12 bytes of preamble, 2 bytes of frame type, 20 bytes of data information, 8 bytes of timestamp, and 2 bytes of marker information. Due to UDP' s unreliability, marker information is added at the frame end to facilitate data reordering and integration after transmission. Excluding transmission information, the data reaches 1,310,720 bits. With an input width of 64 bits and marker information represented by two bytes, complete data transmission requires 20,480 frames. The actual transmission data volume is 1,024 + 44 bytes per frame. shows the detailed byte allocation per frame.

** Frame Data Byte Information Distribution Table**

Byte Position	Data Bit Distribution
0–41	Frame header information
42–1065	Valid data (1024 bytes)
1066–1067	Marker information

Frame spacing is handled as follows: After the Ethernet enable signal is activated and trigger conditions are met, the transmission valid flag becomes 1. Frame header transmission begins and continues until the frame end marker is transmitted. The `tlast` flag appears for one cycle, the MAC core enable signal closes, and counting begins. Based on the count value, timing is calculated according to the PC Client' s reception speed. After testing different speeds, a frame interval of 10 ms is selected to minimize frame loss. After completing one frame transmission, the system enters a waiting state. This waiting has two trigger types: external key trigger and timed trigger. Whichever trigger occurs first restarts the transmission cycle. The specific process is shown in [Figure 1: see original paper].

PC Software Design

After completing the FPGA processing section, data is transmitted via Gigabit Ethernet using UDP. This section describes the work of receiving and processing data on the PC terminal [8].

2.2.1 Data Integrity Detection

The most critical aspect of PC-side data processing is data integrity detection. After asynchronously reading data from the buffer, the first step is length detection. If each frame reaches 1,080 bytes, the next screening step proceeds via frame trailer detection; otherwise, the data is discarded pending the next reception. The last two bytes of the frame trailer are 0x01FF (511). The screening step determines whether information needs processing by detecting the last frame' s trailer information. Since the data contains 20,480 frames, frame counting is performed. If the count reaches 20,480, the process proceeds to the next processing stage; otherwise, data is deleted and the system waits for the next packet. The process principle is shown in [Figure 5: see original paper].

Array sorting reorganizes the obtained 20,480 frames according to their original frame sequence markers. By retrieving the last two bytes of each row and finding the sequence marker, that row is positioned as the corresponding row number, storing only the preceding 1,024 bytes. This requires only 20,480 cycles to perfectly resolve the sorting issue.

2.2.2 Windowing and FFT Design

Windowing is achieved by multiplying the data signal with a window function [9]. FFT processing establishes frequency-domain and time-domain representations.

The butterfly operation implements the transform. First, time-domain data is placed in the complex domain by creating a complex number class. Second, the signal undergoes FFT. Third, the transformed signal' s magnitude is calculated by taking the square root and logarithm to obtain the final result [10]. The X-axis represents frequency, and the Y-axis represents amplitude (dB). [Figure 6: see original paper] shows the PC terminal interface.

Key Metrics Analysis

Due to relatively large low-frequency noise and electromagnetic interference in low-frequency radio observation front-end acquisition, the digital terminal must exhibit excellent performance in spurious-free dynamic range (SFDR) and frequency resolution; otherwise, accurate signal acquisition and analysis are impossible. Because the digital terminal collects high-precision data at high speed, resulting in large data throughput, FFT computation time must also meet stringent requirements to facilitate subsequent storage and analysis.

3.1 Spurious-Free Dynamic Range and Minimum Detectable Signal

SFDR represents a portion of the total dynamic range, defined as the range of input signals where no spurious signals exceed the noise floor when two equal-power signals are input. The receiver' s dynamic range is the usable input signal range, defined as the power level greater than the equivalent noise power within a given IF bandwidth. The standard determining the dynamic range lower limit is called the Minimum Detectable Signal (MDS), which represents the lower bound of the dynamic range.

The theoretical formula is:

$$\mathrm{MDS} = -174\,\mathrm{dBm} + 10\log_{10}(B) + \mathrm{NF}$$

where B is bandwidth and NF is noise figure. The upper limit of SFDR is defined as the input signal level of two equal-level signals that produce third-order intermodulation products equal to MDS. Letting P_u represent the SFDR upper limit and IP represent the receiver' s third-order intercept point, the upper power value is:

$$P_u = \frac{1}{2}(\mathrm{MDS} + IP)$$

The SFDR formula becomes:

$$\mathrm{SFDR} = P_u - P = \frac{1}{2}(IP - \mathrm{NF} - 171\,\mathrm{dBm})$$

With an input intercept point of 10 dBm, noise figure of 6 dB, and sampling frequency of 5 MHz, the theoretical SFDR calculates to 60 dB. The ADS62P49 datasheet gives an SFDR of 59.3 dB, while actual measurement with a 5 MHz signal yields 59.1 dB, confirming the project' s accuracy.

3.2 Frequency Resolution and FFT Computation Time

3.2.1 Frequency Resolution Frequency resolution is the minimum frequency interval obtainable on the frequency axis during discrete Fourier transform. With a sampling frequency of 122.88 MHz and FFT processing of 131,072 points per operation, the frequency resolution is:

$$\Delta f = \frac{122.88\,\text{MHz}}{131072} = 0.9375\,\text{kHz} \approx 0.9\,\text{kHz}$$

Testing with a 5 MHz signal using Matlab shows energy values every 0.9 kHz, fully meeting the system' s minimum frequency resolution requirement of 0.9 kHz. [Figure 7: see original paper] shows the frequency resolution detection.

3.2.2 FFT Computation Time Data is transmitted via Gigabit Ethernet using UDP, with each packet representing one transmission. Each data packet contains 20,480 frames. The inter-frame interval is determined by the UDP Client' s data reception speed. After testing various speeds, a 10 ms frame interval is selected to minimize packet loss. Completing one packet requires 20,480 frames × 10 ms = 204.8 seconds.

FFT processing must be performed after receiving a complete packet. The next packet cannot arrive before FFT processing completes; otherwise, program errors occur. Testing shows FFT computation time is 0.87 seconds, while data storage requires 0.1 seconds. With a packet interval of 204.8 seconds, the timing easily meets requirements. After data storage, received data can be reanalyzed while the next packet transmits.

Far-field signal testing yields the spectrum shown in [Figure 8: see original paper]. A clear peak appears at 59.4 MHz. Compared with observatory data, significant improvements are evident in SFDR, frequency resolution, FFT computation time, and storage.

Conclusion

This system provides a complete solution for low-frequency radio signal reception and observation, primarily implementing Gigabit Ethernet data transmission and FFT spectral analysis. The system has completed testing and is processing actual signals, demonstrating feasibility and reliability. The approach using FPGA and high-speed digital signal processing for radio observations proves effective and will play a significant role in future low-frequency radio astronomy.

References

[1] Zhang Xiyang, He Lesheng, Dong Liang, et al. Design and implementation of a digital observation terminal for solar radio observation within the 800-975 MHz band. *Research & Technology Publications of National Astronomical Observatories of China*, 118-122.

[2] Zhu Kai, Zhang Jian. The FPGA realization of a DDC system based on analytical-signal processing and its application in astronomy. *Astronomical Research & Technology Publications of National Astronomical Observatories of China*, 51–56.

[3] Yu Hai, Fan Xiaoya. Research and implementation of asynchronous FIFO based on FPGA. *Microelectronics & Computer*, 211–212.

[4] Tri-Mode Ethernet Media Access Controller. Xilinx Product Documentation. http://www.xilinx.com/products/intellectual-property/temac.htm

[5] Tri-Mode Ethernet MAC v9.0 LogiCORE IP Product Guide. http://www.xilinx.com/support/documentatio tri-mode-eth-mac.pdf

[6] Wei Hong, Fu Youtao, Kong Fanpeng, et al. Design of gigabit Ethernet system based on FPGA. *Modern Electronics Technique*, 56–59.

[7] Hu Weihua, Hu Xixiang. Network protocol analysis and implementation. *Higher Education Press*, 155–156.

[8] Liu Guangchen, Zhang Huian, Jia Aibin. Study on the window-adding problem in digital signal processing. *Journal of Changsha University*, 59–63.

[9] Shi Hao. The implementation of FFT on C#. http://blog.sina.com.cn/s/blog_4b3107860100xdvu.html

[10] Spurious-free dynamic range—factors affecting communication equipment performance. *Fujian Computer*, 99–103.

Note: Figure translations are in progress. See original paper for figures.