Optimal Loop Bandwidth Selection for Phase-Locked Frequency Synthesizers (Postprint)

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Abstract

The selection of loop bandwidth values for phase-locked loop frequency synthesizers directly affects their output phase noise. Based on this, this paper first introduces the basic components of phase-locked loops, then analyzes the impact of phase noise from crystal oscillators, integrated PLL chips, and voltage-controlled oscillators on the noise at the output of the frequency synthesizer loop, thereby deriving a calculation formula for the optimal loop bandwidth. Furthermore, the correctness of the optimal loop bandwidth formula was verified through output phase noise measurements of a frequency synthesizer based on the PE3236 chip. The results show that when the values are taken according to the optimal loop bandwidth formula, the output phase noise of the phase-locked loop frequency synthesizer meets the requirements of practical applications.

Full Text

Selection of Optimal Loop Bandwidth for PLL Frequency Synthesizers

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Abstract

The selection of loop bandwidth for phase-locked loop (PLL) frequency synthesizers directly influences output phase noise performance. This paper first introduces the fundamental components of PLLs and then analyzes how phase noise from the crystal oscillator, integrated PLL chip, and voltage-controlled oscillator (VCO) affects the output noise of the frequency synthesizer loop, leading to the derivation of an optimal loop bandwidth calculation formula. The validity

of this formula is verified through output phase noise measurements of a frequency synthesizer based on the PE3236 chip. Results demonstrate that when the loop bandwidth is set according to the proposed formula, the PLL frequency synthesizer' s output phase noise meets practical application requirements.

Keywords: Phase-locked loop; Frequency synthesizer; Loop bandwidth; Phase noise
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Introduction

In communication systems, PLL frequency synthesizers represent a primary method for generating local oscillator frequencies [1]. This approach offers advantages including high spectral purity and wide frequency range, making it widely applicable in communications, aerospace, and telemetry technologies as the mainstream frequency synthesis technique today. Loop output phase noise constitutes one of the key technical specifications of PLL frequency synthesizers, directly impacting overall communication system performance [2]. Therefore, this paper derives a loop bandwidth formula for selecting optimal bandwidth values through analysis of two types of noise affecting loop output, and experimentally verifies the formula' s applicability for frequency synthesizer loop bandwidth selection.

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Phase-Locked Loop Phase Noise Model

A phase-locked loop [3] (PLL) is a circuit that enables external reference signals to control the frequency and phase of an internal oscillator, functioning as a phase feedback control system. The PLL architecture consists of four main components: phase detector, low-pass filter, voltage-controlled oscillator (VCO), and frequency divider.

In PLL frequency synthesizers [4], numerous noise sources exist. For practical applications, these noises are typically treated as external inputs. The equivalent noise from active devices in the loop filter is relatively small compared to other noise sources and can be neglected. The loop phase noise model of the PLL frequency synthesizer is shown below.

[Figure 1: see original paper]

As illustrated above, phase noise sources in PLL frequency synthesizers are categorized into two types: low-pass phase noise and high-pass phase noise. Low-pass phase noise originates from the temperature-compensated crystal oscillator (TCXO) and internal triggers within the integrated PLL chip.

The integrated PLL chip noise primarily comprises trigger phase noise from digital dividers and phase detector trigger phase noise. Since phase noise from the PLL frequency synthesizer accumulates at the output, the crystal oscillator'

s frequency can be viewed as being multiplied and then phase-detected with the VCO frequency. The resulting multiplied crystal oscillator phase noise is comparable to the internal phase noise of the integrated PLL chip, making the crystal oscillator' s contribution to PLL output phase noise non-negligible.

High-pass phase noise is typically referred to as oscillator noise. In this PLL, the VCO phase noise consists mainly of flicker noise and thermal noise.

Because the power of both low-pass and high-pass noise is far smaller than the signal power, their effects on signal noise spectral density can be approximated as independent. Consequently, the output phase noise spectral density [6] can be expressed as:

$$S_{\phi o}(\omega) = S_{\phi l0}(\omega) + S_{\phi h0}(\omega)$$

where $S_{\phi l0}(\omega)$ represents the phase noise spectral density at the loop output due to combined effects of the crystal oscillator and triggers, and $S_{\phi h0}(\omega)$ represents the phase noise spectral density at the loop output due to the VCO. Generally, low-pass noise energy concentrates primarily in the low-frequency region. When the loop bandwidth is narrow [7], the following formula applies.

The phase noise spectral density of the crystal oscillator and integrated PLL chip [8] can be expressed as:

$$S_{\phi r}(\omega) + S_{\phi j}(\omega) = h_{\omega r}^{-1} + 4\pi\sigma^2\Delta t R\omega_r$$

The VCO phase noise spectral density can be expressed as:

$$S_{\phi v}(\omega) = h_{-1}^{v}\omega^{-3} + h_0^v\omega^{-2} + h_1^v\omega^{-1} + h_2^v\omega^0 \approx h_{-1}^{v}\omega^{-3}$$

where h_{-1}^{v}, h_0^v, h_1^v, and h_2^v are the power-law coefficients for the VCO' s flicker noise FM spectrum, white noise FM spectrum, flicker noise PM spectrum, and white noise PM spectrum, respectively. In practice, the flicker noise FM spectrum dominates the VCO noise spectrum, allowing the last three terms to be neglected.

Optimal Loop Bandwidth

When the PLL employs a high-gain second-order loop filter, the magnitude-frequency characteristics of the overall loop transfer function become:

$$|H_l(j\omega)|^2 = \frac{4 + 2\omega_n^2 + 4\varepsilon^2\omega^2}{2(2\varepsilon^2 - 1)\omega^2 + \omega^4}$$

$$|H_h(j\omega)|^2 = \frac{2(2\varepsilon^2 - 1)\omega^2 + \omega^4}{4 + 2\omega_n}$$

where $|H_l(j\omega)|^2$ and $|H_h(j\omega)|^2$ represent the output magnitude-frequency characteristics of the loop when low-pass and high-pass phase noise act separately, and ε and ω are the damping coefficient and loop natural resonant frequency [9].

From the loop output phase noise variance formula:

$$\phi_o = \frac{1}{2\pi}\int S_{\phi o}(\omega)|H(j\omega)|^2 d\omega$$

Substituting the above formulas into the loop output phase noise variance formula yields:

$$\phi_{ro} + \sigma^2\phi_{ro} = \frac{1}{2\pi}\int (S_{\phi r}(\omega)|H_l(j\omega)|^2 + S_{\phi j}(\omega)|H_l(j\omega)|^2)d\omega = h^2 B_L \quad (8)$$

$$\phi_{vo} = \frac{|H_h(j\omega)|^2 d\omega}{2\pi}\int S_{\phi v}(\omega)\frac{h_{-1}^v \omega d\omega}{2(2\varepsilon^2-1)\omega^2+\omega^4}\frac{4+2\omega_n}{h_{-1}^v(4\varepsilon^2+1)^2\pi(8\varepsilon)^3 B_L}\frac{2\sqrt{\varepsilon^2-1}}{\ln[(2\varepsilon^2-1)+2\varepsilon\sqrt{\varepsilon^2-1}]}\frac{h_{-1}^v(4\varepsilon^2+1)}{\pi(8\varepsilon)^3\sqrt{\varepsilon^2-}}$$

This yields the following expression:

$$\phi_o = h^2 B_L + \frac{M}{B_L}$$

$$B_L = \sqrt{\frac{2(4\varepsilon^2+1)^2}{\pi(8\varepsilon)^3\sqrt{\varepsilon^2-1}\ln[(2\varepsilon^2-1)+2\varepsilon\sqrt{\varepsilon^2-1}]}}$$

When the loop bandwidth reaches a certain value, the loop output phase noise variance reaches its minimum, making this frequency point the optimal loop bandwidth. When the damping coefficient is selected between 1 and 1.5, this optimal bandwidth value [10] is:

$$B_L = ($$

Experimental Verification

This experiment was conducted using a PLL frequency synthesizer based on the PE3236 chip. By directly measuring the 10 MHz TCXO phase noise and adding the trigger phase noise provided in the chip datasheet, the resulting phase noise spectral density near the loop phase noise appears as $S_{\phi r}(\omega) = h^2\omega^{-1} = 1\times10^{-11}\omega^{-1}$. Measuring the VCO with a center frequency of 1.5 GHz yields a phase noise spectral density of $S_{\phi rv}(\omega) = h_{-1}^v\omega^{-3} = 6.1918\omega^{-3}$.

Substituting these approximate values into the optimal loop bandwidth calculation formula gives a loop bandwidth value of 62.8 kHz.

To verify the correctness of the approximate loop bandwidth calculation formula [11], we employed a direct measurement method to select the optimal loop bandwidth. Using this method, we first measured the low-pass and high-pass phase noise power spectral curves separately [12], then compared the intersection frequency with the value obtained from the calculation formula. When the PLL loop bandwidth is set very wide, the measured spectrum within the loop bandwidth consists primarily of the low-pass noise power spectral curve. When the loop bandwidth is made very narrow, the measured loop output phase noise corresponds to the high-pass phase noise power spectral curve [13]. Figures (a) and (b) show the PLL output frequency phase noise for loop bandwidths of 300 kHz and 3 kHz, respectively. The characteristic feature is that when the loop bandwidth is at the intersection point of the two curves, the loop bandwidth is optimal, which occurs at approximately 63 kHz. For more illustrative purposes, the PLL loop bandwidth was set to 65 kHz, as shown in figure (c) below. For comparative illustration, the measured results are contrasted in Figure 3 [Figure 3: see original paper].

[Figure 2: see original paper]

Verification confirms that the optimal loop bandwidth value for the PLL is approximately equal to the value calculated by the formula. Measurement errors in VCO phase noise spectral density are typically large [14], so the intersection value is obtained approximately, but this does not affect the determination of the optimal loop bandwidth.

Conclusion

The optimal loop bandwidth of PLL frequency synthesizers represents an effective measure for improving signal quality [15]. Through testing and analysis of output phase noise from a PE3236-based PLL frequency synthesizer, the theoretical values from the optimal loop bandwidth calculation formula show good agreement with actual measured values. Therefore, the optimal loop bandwidth value obtained from the calculation formula can be reliably applied to loop bandwidth selection for local oscillator frequency sources in various equipment.

Experimental findings indicate a certain difference between the multiplied crystal oscillator phase noise and the internal phase noise of the integrated PLL chip. As the integrated circuit industry continues to develop, internal noise in integrated PLL chips used in frequency synthesizers is gradually being reduced, making crystal oscillator phase noise more prominent in its effect on the near-carrier output frequency of PLL frequency synthesizers, exhibiting a bump phenomenon. Consequently, selecting high-performance crystal oscillators plays an important role in determining frequency synthesizer output phase noise.

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Note: Figure translations are in progress. See original paper for figures.