Postprint: Research on Terahertz Interferometer System Based on High-Speed Digital Correlator

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Abstract

Interferometers utilize inter-channel correlation operations for measurement and constitute the fundamental unit of interferometric imaging. Terahertz imaging holds broad application prospects in security screening, military reconnaissance, and other domains. Following the introduction of interferometric imaging measurements into the terahertz field, to address the phase synchronization problem of high-speed signals in correlation operations, this paper proposes a cross-synchronization scheme based on low-speed FPGA control, which solves the phase synchronization issue of high-speed sampling signals at low hardware cost, and implements a multi-channel high-speed digital correlation system. The system' s maximum sampling rate is 5 GHz, the ADC effective number of bits is greater than or equal to 6 bits, and the correlator integration time is adjustable. Finally, using this digital correlator and corresponding terahertz microwave components, an interferometer with a center frequency of 0.44 THz was constructed, and clear interference fringes were obtained with a linear phase error of less than 2°. This research provides a basic unit for the future design of terahertz interferometric imagers.

Full Text

Investigation of a THz Interferometer System Based on High-Speed Digital Correlators

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Abstract: The interferometer, which performs measurements through correlation operations between channels, constitutes the fundamental unit of interferometric imaging. Terahertz imaging exhibits broad application prospects in security screening and military reconnaissance. After introducing interferometric imaging measurements into the terahertz domain, this paper proposes a cross-synchronization scheme controlled by a low-speed FPGA to address the phase synchronization challenge in high-speed signal correlation operations, achieving this with minimal hardware cost. A multi-channel high-speed digital correlation system has been completed with a maximum sampling rate of 5 GHz, ADC effective number of bits 6, and adjustable correlator integration time. Finally, an interferometer with a center frequency of 0.44 THz was constructed using this digital correlator and corresponding terahertz microwave components, yielding clear interference fringes with a linear phase error of less than 2°. This research provides a fundamental building block for future terahertz interferometric imager design.

Keywords: Terahertz; Interferometric imaging; High-speed digital correlator; Phase synchronization

1 Introduction

The terahertz frequency band lies between microwave and infrared. Due to the excellent penetration capability of terahertz electromagnetic waves through most non-metallic and non-polar media, passive terahertz imaging technology holds tremendous application potential in anti-terrorism security screening and military reconnaissance [1]. Particularly in military reconnaissance, passive terahertz imaging can operate effectively in adverse weather conditions compared to conventional optical and infrared imaging. Furthermore, unlike active radar systems, passive imaging methods do not require electromagnetic wave transmission, offering better concealment [2].

Current millimeter-wave and submillimeter-wave terahertz imaging can be categorized by imaging architecture into mechanical scanning, focal plane imaging, interferometric synthetic aperture imaging, and phased array beamforming. Phased array technology faces significant engineering implementation challenges and limited applications due to device limitations, system cost, and power consumption constraints. Real-aperture mechanical scanning systems [3] feature simple principles and low cost but suffer from low imaging rates, with system performance heavily dependent on mechanical platform stability. Focal plane array imaging [4] represents the most widely adopted passive millimeter-wave imaging architecture, primarily because the processing precision and performance of antennas, feeds, and MMIC receivers for this architecture have improved substantially in recent years. Its main drawback lies in the numerous receiver systems required, leading to high complexity and cost. Interferometric synthetic aperture technology [5] employs effective sparse antenna arrays for frequency-

domain measurements to replace time-domain measurements. This technology first achieved successful application in radio astronomy [6] and subsequently expanded into microwave remote sensing, playing important roles in Earth observation—exemplified by NASA' s ESTAR airborne radiometer [7], ESA' s SMOS satellite MIRAS microwave radiometer [8], and the GIMS geostationary microwave radiometer prototype from the National Space Science Center, Chinese Academy of Sciences [9-10], all of which successfully utilized interferometric synthetic aperture imaging. The primary advantage of interferometric imaging compared to other methods is its elimination of mechanical scanning and high-precision parabolic antennas; high spatial resolution and sensitivity images can be obtained through synthesis of data from distributed small antennas, with antenna array element count minimized through optimal baseline design.

The challenge in terahertz interferometric imaging lies in preserving terahertz signal phase information for complex correlation operations. This paper proposes a high-speed digital correlator that performs digital sampling directly in the intermediate frequency band, employing a cross-synchronization scheme to ensure phase synchronization of high-speed signals. Based on system logic resource and processing speed requirements, Xilinx V6 series FPGAs were selected for real-time correlation operations [11], completing the entire high-bandwidth digital correlator architecture. Subsequently, a 0.44 THz two-element interferometer was constructed using independently developed terahertz antennas and receivers from the National Space Science Center [12] together with this digital correlator, yielding point-source interference fringes. This terahertz interferometer serves as a fundamental unit for future terahertz interferometric imager design.

2 Interferometric Imaging Principle

The two-element interferometer constitutes the fundamental unit of interferometric imaging [6], with its basic model shown in Figure 1

. Assuming plane wave incidence, the Q-channel output for a system observing a monochromatic point source at inclination angle is:

$$Q = \langle V_g(t) \cdot V_g(t-\tau) \rangle = \frac{A^2}{2} \cos(2\pi f_0 \tau) = \frac{A^2}{2} \cos\left(\frac{2\pi D \sin\theta}{\lambda}\right) \qquad (1)$$

where $\langle \cdot \rangle$ denotes temporal expectation, λ is the wavelength of the monochromatic point source, A characterizes the source' s radiation intensity, and $\tau = D\sin\theta/c$ represents the time delay. Equation (1) represents the mathematical expression of interference fringes for a two-element interferometer.

Extending the point source to a line source and letting $\xi = \sin\theta$, the system response to a monochromatic line source can be viewed as the linear superposition of infinite monochromatic point source responses:

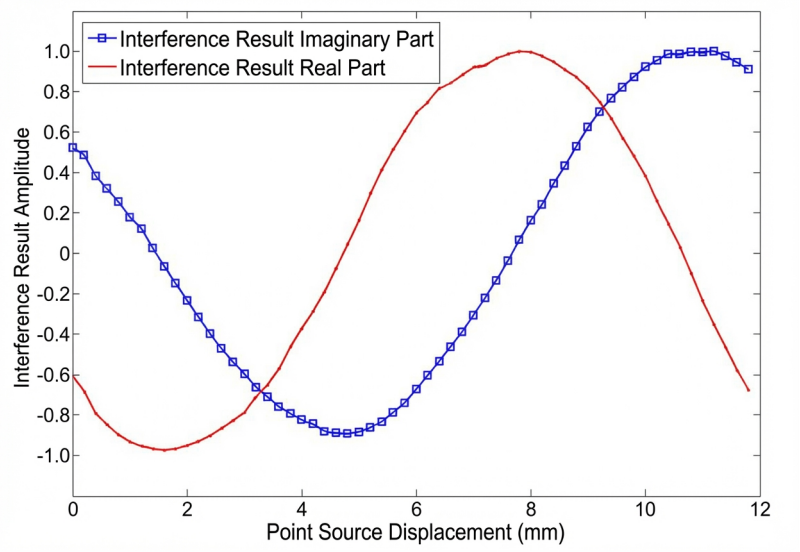

Figure 1: Figure 1

$$Q = \int T(\xi) \cos\left(\frac{2\pi D\xi}{\lambda}\right) d\xi \tag{2}$$

The Fourier transform expression is:

$$V(u) = \int T(\xi) e^{-j2\pi u\xi} d\xi \tag{3}$$

The Q-channel output of the system shown in Figure 1 corresponds to the real part of the Fourier transform of $T(\xi)$ evaluated at $u = D/\lambda$. Similarly, the I-channel output yields the imaginary part. With numerous two-element interferometers of varying spacings, a discrete expression of the Fourier transform function $V(u)$ can be obtained, enabling reconstruction of $T(\xi)$. This constitutes the fundamental principle of interferometric radiometer imaging, demonstrating that the two-element interferometer is the basic unit of interferometric imaging measurements. In practical systems, the signal is typically not monochromatic but band-limited Gaussian white noise constrained by receiver filters H_1 and H_2, requiring consideration of the fringe-washing function' s effects [13].

3 THz Interferometer System Architecture

The THz interferometer primarily comprises three subsystems: antenna, submillimeter-wave front-end, and digital correlator. The system block

diagram is shown in Figure 2 [FIGURE:2].

The antenna subsystem handles signal acquisition and reception. Horn antennas were selected for this system due to their mature technology, high gain, low VSWR, wide operating bandwidth, simple structure, ease of manufacturing, and high reliability. After fabrication and testing, the antenna achieved 25.6 dB gain, 10° 3-dB beamwidth, and -30 dB sidelobe level, meeting design requirements.

The submillimeter-wave front-end employs a second-harmonic mixing scheme, primarily consisting of a common local oscillator, power divider, frequency tripler, and mixer. The frequency tripler plays a crucial role in generating sufficient in-phase terahertz power [12]. The intermediate frequency signal after harmonic mixing is fed directly into the high-speed digital correlator for subsequent processing.

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4 Design and Implementation of High-Speed Digital Correlator for THz Interferometer

The intermediate frequency signal input to the digital correlator undergoes analog-to-digital conversion, digital quadrature down-conversion, and complex correlation operations to obtain raw interferometric measurements, which are then stored or uploaded to a PC for real-time processing.

Structurally, the digital correlator comprises analog-to-digital conversion, digital quadrature down-conversion, digital complex correlation, and data storage/processing units. The detailed architecture is shown in Figure 3 [FIGURE:3].

The clock generation and distribution module provides synchronized sampling clock sources for multiple ADC modules. The ADC module digitizes the intermediate frequency signal. The data processing module handles intermediate frequency digital signals to produce correlation outputs. The control and data interface module configures parameters for all modules and exports data.

4.1 Clock Generation and Distribution Module

The clock generation module employs an ADF4350 PLL chip to multiply a 10 MHz active crystal oscillator, followed by distribution using an ADCLK944 chip. Clock quality in the sampling clock network significantly impacts system performance, with clock phase jitter being a critical evaluation metric. Sampling clock jitter causes sampling point deviations, primarily degrading ADC conversion SNR and reducing effective number of bits [14].

The relationship between ADC channel SNR and clock signal RMS jitter σ is typically expressed as:

$$\mathrm{SNR} = 20\log_{10}\left(\frac{1}{2\pi f_{\mathrm{in}}\sigma}\right) \tag{4}$$

where f_{in} is the analog input frequency. The relationship between ADC channel SNR and effective number of bits (ENOB) is:

$$\mathrm{ENOB} = \frac{\mathrm{SNR} - 1.76}{6.02} \tag{5}$$

For the ADC module in this correlator, the maximum system sampling rate is 5 GHz with 8-bit conversion. The system requirement specifies an effective number of bits 6, yielding a required clock jitter $<$ 7.82 ps. The ADF4350 exhibits typical RMS jitter of 0.5 ps, while the ADCLK944 contributes 0.05 ps RMS. Post-implementation testing confirmed the clock generation and distribution system' s RMS jitter meets performance requirements.

4.2 High-Speed Analog-to-Digital Conversion Module

High-speed analog-to-digital conversion is prerequisite for high-speed correlation. Higher conversion rates ensure adequate correlation operation bandwidth and sensitivity.

The ADC module' s core component is the e2v ev8aq series chip, containing four ADC cores configurable in three modes: 5 GHz single-channel, 2.5 GHz dual-channel, or 1.25 GHz quad-channel operation. Additionally, different digital sampling frequencies can be obtained by configuring the ADF4350 multiplication factor in the clock generation module. System testing verified ADC effective bits 6, meeting requirements [14].

4.3 Data Processing Module

The data processing module handles intermediate frequency digital signals, comprising digital quadrature down-conversion and correlation processing submodules.

Each channel feeds into a digital quadrature down-conversion module [15], which sequentially includes a bandpass filter, quadrature mixer, and low-pass filter. Significant bit-width expansion occurs when signals pass through filters and multipliers, necessitating truncation optimized based on input signal amplitude range and spectral characteristics. For parallel data streams generated by high-speed sampling, parallel FIR filter design enables parallel signal filtering [15].

The correlation processing module includes autocorrelation, auto-accumulation, and cross-correlation operations. Autocorrelation functions as total power detection for channel power estimation. Auto-accumulation estimates ADC quantization threshold errors and offset [16]. Cross-correlation yields raw interferometric measurements. Each channel connects to an autocorrelation/auto-accumulation

module, with all channel pairs performing cross-correlation. Cross-correlation consumes the most resources; to conserve resources, each channel' s data undergoes three-level requantization before cross-correlation [17]. The three-level requantization covariance coefficient has a fixed conversion relationship with the analog correlation coefficient, equivalent to integration time loss [17-18].

4.4 Control and Data Interface Module

System parameters including clock module multiplication factor, ADC operating mode, and correlation integration time can be configured via host computer. The controller employs an AXI_lite bus master within the FPGA, with all system units serving as AXI_lite slaves. Correlation module data is transmitted in AXI_stream format to the communication interface conversion module, then uploaded to the PC via USB after conversion.

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5 Phase Synchronization Implementation

5.1 Phase Synchronization Error Source Analysis

Interferometer receiver channels typically require multiple ADC chips for synchronous sampling, necessitating resolution of high-speed inter-ADC coordination issues. For the ev8aq chip, inter-chip ADC sampling phase differences primarily comprise two components: phase difference introduced by frequency division ambiguity, and phase difference caused by varying channel delay lines.

In this system, the four ADC cores within each ev8aq chip derive their sampling clocks from external input sampling clocks through frequency division, creating potential inter-chip division ambiguity. Additionally, practical system tolerances cause path delay variations from ADF4350 to multiple ev8aq chips, inevitably introducing phase differences in the actual input clocks.

5.2 ADC Sampling Clock Phase Error Correction

Division ambiguity-induced phase difference fundamentally stems from asynchronous operation among multiple ev8aq chips. The ev8aq chip features dedicated synchronization pins for inter-chip synchronization, with its data output clock sharing the same source as the sampling clock. Leveraging this functionality, this paper proposes a cross-synchronization scheme. The implementation method is: first, provide an arbitrary synchronization signal to one ev8aq chip (designated 'a') to obtain its output data clock; then use this output data clock to synchronize another ev8aq chip (designated 'b'), establishing b in a determined mode; finally, use b' s output data clock to synchronize all remaining ev8aq chips, bringing all chips into synchronization with b' s mode. The control logic is shown in Figure 4 [FIGURE:4].

For phase differences introduced by varying channel delay lines, the situation

is complex, encompassing both clock network delay differences and analog signal network delay differences, with additive effects. The ev8aq chip provides per-ADC-core programmable delay lines for sampling edges with 110 fs adjustment resolution, enabling further improvement of inter-chip and intra-chip ADC sampling timing precision.

5.3 ADC Synchronization Status Monitoring

Each chip' s data clock is derived from the actual ADC sampling clock through frequency division. Monitoring phase differences among these data clocks enables evaluation of ADC synchronization status. Using Monte Carlo analysis, phase differences between data clocks are converted to probabilities of random events, then statistically analyzed through extensive experiments. The implementation logic is shown in Figure 4 [FIGURE:4].

Since all data clocks share the same source, their phase difference $\delta\psi$ can be assumed constant. When randomly sampling these two clock signals, the probability P_{equ} of identical sampling results relates to $\delta\psi$ as:

$$P_{\text{equ}} = 1 - \frac{|\delta\psi|}{\pi} \tag{6}$$

Sampling the two clocks with an unrelated clock and statistically analyzing numerous results enables estimation of P_{equ}. In practice, after cross-synchronization, $P_{\text{equ}} < 0.004$, corresponding to $|\delta\psi| < 0.72°$. This value includes errors from the test method and FPGA internal routing, providing confidence that the ev8aq modules have achieved synchronous operation. Without cross-synchronization, $P_{\text{equ}} > 0.1$, indicating asynchronous ev8aq operation.

5.4 ADC Consistency Testing

Following ADC synchronization via the cross-synchronization scheme, ADC consistency was tested. ADC consistency, related to sampling clock network, ADC performance, and analog signal network, is critical for interferometer phase extraction. Single-frequency test signals were applied to each ADC' s analog input for consistency testing, with sampled quantization results analyzed.

Direct time-domain comparison of inter-channel inconsistencies is difficult. After applying Fourier transform to each ADC' s sampled quantization results, phase differences at peak frequency points in the frequency domain estimate inter-channel time delay errors. Testing revealed intra-chip channel consistency superior to inter-chip consistency, with inter-chip channel consistency 20 ps and intra-chip channel consistency 10 ps, meeting system performance requirements.

6 Experimental Verification

6.1 Experimental System Configuration

Point-source interference experiments were conducted using the described THz interferometer and corresponding point noise source. This research introduces interferometric measurement technology into the terahertz domain, obtaining clear terahertz interference fringes and linear interferometric phase, providing important reference value for future terahertz interferometric measurement and imaging.

For THz imaging, frequency band selection must consider multiple factors. Lower frequencies yield lower imaging resolution due to antenna aperture limitations, while higher frequencies, though enabling desirable resolution with smaller apertures, suffer from scattering attenuation by clothing and other obscurants in security and reconnaissance applications [4]. Additionally, to maximize THz detection advantages, frequency band design should consider the terahertz radiation spectra of sensitive objects like metals and ceramics in security screening. Balancing these factors, this interferometer selected 440 GHz as the operating frequency for use as a fundamental unit in future THz interferometric imagers.

The experimental system includes the THz interferometer described herein, control and data processing host computer, point noise source, and sliding rail mechanical frame for noise source positioning. The experimental block diagram is shown in Figure 5 [FIGURE:5], with the rail parallel to the interferometer baseline, enabling precise point-source movement along the baseline direction.

During measurement, the noise source was precisely positioned using the sliding rail (position accuracy < 3 m). Two antenna receivers operated in the 440 GHz band with an interferometer baseline of 59.52 mm and baseline-to-rail distance of 1100 mm. After first down-conversion, signals entered the digital correlator, undergoing digital quadrature down-conversion and digital correlation before results were transmitted to the host computer for analysis at different noise source positions.

6.2 Experimental Data Analysis

After calibration correction, the real and imaginary parts of the obtained correlation data were plotted against noise source position to produce interference fringes, shown as the two curves in Figure 6 FIGURE:6. Since the point noise source distance far exceeds the terahertz signal wavelength, Equation (1) indicates a linear relationship between interferometric result phase and source displacement. Extracting phase from each point in Figure 6(a) yields the interferometer' s linear phase plot, shown in Figure 6 FIGURE:6.

According to Equation (1), the displacement corresponding to one interference fringe period at the phase center 1100 mm away is 12.6 mm, while the measured

value is 12.4 mm, achieving the expected accuracy. Linear phase error is $< 2°$, demonstrating normal interferometer operation within expected precision.

7 Conclusion

This paper addresses high-speed digital sampling synchronization issues through a cross-synchronization method among multiple high-speed ADC chips, implementing a high-speed digital correlation system that integrates analog-to-digital conversion, quadrature down-conversion, and correlation operations on a single digital backend. A novel and straightforward method monitors consistency across ADC channels. Testing demonstrated inter-chip channel consistency 20 ps and intra-chip channel consistency 10 ps, satisfying direct sampling requirements in the GHz band.

Additionally, this paper proposes a THz interferometer based on the high-speed digital correlation system and corresponding millimeter-wave components. Interferometric measurements of a point noise source at 0.44 THz yielded clear interference fringes and linear phase (Figure 6) with linear phase error $< 2°$. This interferometer provides a fundamental unit for future THz interferometric imager design.

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