Research on Frequency Synthesis Circuit Based on PE3236 Chip (Postprint)

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Date: 2017-03-10T00:00:00+00:00

Abstract

This paper presents a design scheme for a phase-locked frequency synthesizer circuit applied to L-band. A phase-locked loop circuit design based on the PE3236 chip is presented. Through simulation verification and experimental results, the relationship between phase-locked loop bandwidth, loop output phase noise, and loop acquisition time is discussed in detail. Experimental results show that this scheme can be applied to the RF front-end of navigation receivers; the frequency synthesizer circuit exhibits stable performance and meets practical application requirements.

Full Text

Research on Phase-Locked Loop Frequency Synthesis Circuit Based on PE3236

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Abstract: This paper presents a design scheme for a phase-locked frequency synthesizer applied in the L-band. The phase-locked loop (PLL) circuit design based on the PE3236 chip is proposed, with emphasis on the relationship between PLL loop bandwidth and both loop output phase noise and loop acquisition time through simulation verification and experimental results. Experimental results demonstrate that this scheme can be applied to the RF front-end of navigation receivers, exhibiting stable performance and meeting practical application requirements.

Keywords: Phase-Locked Loop; Frequency Synthesizer; Loop Bandwidth; Phase Noise; Acquisition Time

Chinese Classification Number: TP302
Document Identification Code: A

In communication systems [**?**], methods for generating variable local oscillator frequencies include frequency multiplication, direct digital frequency synthesis, and phase-locked loop technology. Frequency multiplication suffers from large spurious components and difficult harmonic suppression, while direct digital frequency synthesis devices operate at relatively low frequencies with high power consumption. In contrast, phase-locked loop technology offers advantages such as simple structure, high spectral purity of output frequency, and wide frequency range, making it widely applied in communications, radar, aerospace, and telemetry fields as the mainstream frequency synthesis technology today. The primary technical specifications for frequency synthesis circuits employing PLL technology [**?**] are loop output phase noise and loop acquisition time, which directly impact overall communication system performance. Therefore, this paper designs a phase-locked frequency synthesizer circuit for L-band applications and verifies the relationship between loop bandwidth and both loop output phase noise and loop acquisition time through preliminary simulation analysis and circuit measurement results.

2.1 Design Performance Specifications

Based on design requirements, the PLL performance specifications are: (1) Frequency: 1 GHz–2 GHz; (2) Power: 12 ± 1 dBm; (3) Single-sideband phase noise: –70 dBc/Hz @ 100 Hz offset; (4) Acquisition time: 10 ms.

2.2 Scheme Design

According to the design specifications and the high requirements for circuit size and power consumption, the selected scheme employs the PE3236 chip with integrated phase detection and frequency division functions, combined with an external active second-order low-pass filter [**?**] and a VCO module suitable for L-band operation. This configuration enables the PLL output frequency to achieve low phase noise while facilitating convenient adjustment of the active second-order low-pass filter parameters for flexible loop bandwidth [**?**] selection. The system block diagram is shown below.

[FIGURE:2] Scheme design block diagram
[FIGURE:1] System block diagram

When the phase-locked loop is locked, the loop bandwidth is given by:

$$\omega_n = \sqrt{\frac{NR_1C_1}{\omega_n R_2 C_2}}$$

where K_d is the phase detector sensitivity, K_v is the VCO sensitivity, N is the frequency division ratio, and R_1, R_2, C_1, C_2 are the loop filter parameter values. ε represents the system damping coefficient.

The active second-order loop low-pass filter [**?**] ensures that the cutoff frequency remains independent of load variations while providing better stability compared to passive low-pass filters. The second-order loop low-pass filter offers optimal phase margin and high stability. Additionally, considering the wide output frequency band of the loop, if the VCO input voltage exceeds the phase detector output voltage, the active circuit can achieve DC voltage amplification.

2.3 Phase Noise Analysis

Phase noise [**?**] is one of the most critical metrics for phase-locked frequency synthesizers, characterizing the short-term stability of the output frequency under various noise sources within the PLL system. Phase noise is typically analyzed in the frequency domain and described through single-sideband noise power spectral density.

Phase noise sources in PLL systems [**?**] include the reference source, phase detector, VCO, and frequency divider. Since externally introduced noise cannot be accurately estimated, the analysis focuses on the impact of internal loop components. To accurately evaluate phase noise performance, a phase noise model for the PLL is established [**?**] as shown below. The noise contributions from the reference source, phase detector, VCO, and frequency divider are represented by S_{ref}, S_{pd}, S_{vco}, and S_n, respectively, with the total loop output noise denoted as S_{tot}:

$$S_{tot} = \left(S_{ref}^2 + S_n^1 + \frac{G(S)}{N} + S_{pd}^1 + \frac{G(S)}{N} + S_{vco}^1 + \frac{G(s)}{N} \right)$$

where $G(s) = F(S)K_dK_v$. Based on the above equation combined with loop bandwidth analysis, when $\omega \gg \omega_c$, $G(s) \to 0$; when $\omega \ll \omega_c$, $G(s)$ dominates. Therefore, by extracting common factors from the equation, the following relationships exist [**?**]:

$$S_{tot} = (S_{ref}^2 + S_n^2 + S_{pd})\{N\}^2 + S_{vco} \quad (\omega \ll \omega_c)$$

$$S_{tot} = S_{vco}$$

Consequently, within the loop bandwidth, the loop provides limited suppression of noise generated by the reference source, phase detector, loop filter, and frequency divider, while significantly suppressing noise from the VCO [**?**]. The opposite holds true outside the loop bandwidth. During design, the loop bandwidth should be reasonably selected based on actual loop conditions [**?**].

2.4 Acquisition Time

The time required for the loop to transition from an initial unlocked state to a locked state is defined as the loop acquisition time. The capture range $\Delta\omega$ represents the maximum initial frequency difference that the loop can pull in and achieve lock through frequency 牵引. Therefore, to improve acquisition performance, the loop bandwidth can be increased to reduce acquisition time. However, increasing the loop bandwidth will also increase loop output phase noise. Thus, in practical design, a trade-off must be made in selecting loop parameters.

3.1 Simulation Analysis

Using ADS simulation software, a PLL frequency synthesizer circuit model was established to simulate and verify the relationship between loop bandwidth and both phase noise and acquisition time.

3.1.1 Relationship Between Loop Bandwidth and Phase Noise Using the loop bandwidth formula and the control variable method, loop bandwidth parameters were varied to observe changes in phase noise. By modifying the active low-pass filter parameters, loop bandwidths of 100 kHz, 50 kHz, and 10 kHz were set to observe variations in loop output phase noise.

[FIGURE:3] Phase noise simulation diagram for loop bandwidths of 100 kHz, 50 kHz, and 10 kHz

Comparing the three diagrams reveals that loop bandwidth is closely related to loop output phase noise magnitude. Both excessively large and excessively small loop bandwidth values result in poor overall noise suppression performance, and each loop has an optimal bandwidth that minimizes loop output phase noise power [**?**].

3.1.2 Relationship Between Loop Bandwidth and Acquisition Time Using the loop bandwidth formula and the control variable method, loop bandwidth parameters were varied to observe changes in acquisition time. By modifying the active low-pass filter parameters, loop bandwidths of 100 kHz, 50 kHz, and 10 kHz were set to observe differences in loop acquisition time.

[FIGURE:4] Acquisition time simulation diagram

Loop acquisition time for bandwidths of 100 kHz, 50 kHz, and 10 kHz

Comparison of the three diagrams shows that larger loop bandwidth results in shorter acquisition time and better acquisition performance, while smaller loop bandwidth leads to longer system acquisition time and poorer acquisition performance. Therefore, selecting an appropriate loop bandwidth significantly impacts both loop output phase noise and loop acquisition time, making a moderate intermediate value ideal for optimal loop bandwidth selection [**?**].

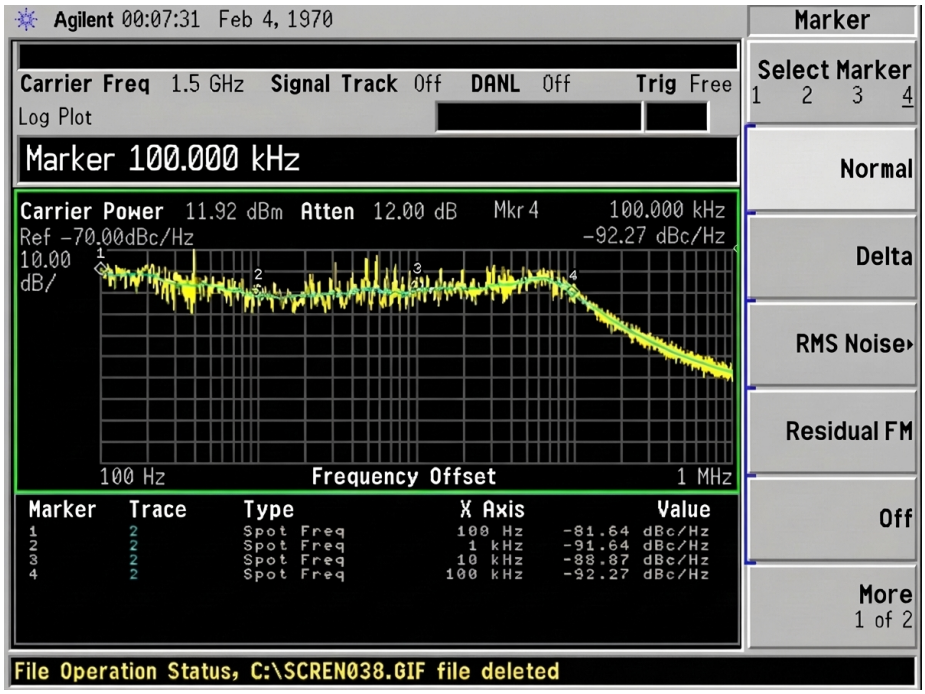

Figure 1: Figure 5

3.2.1 Output Phase Noise Testing

Phase noise measurements were conducted at a loop output frequency of 1.5 GHz with loop bandwidths set to 100 kHz, 50 kHz, and 10 kHz.

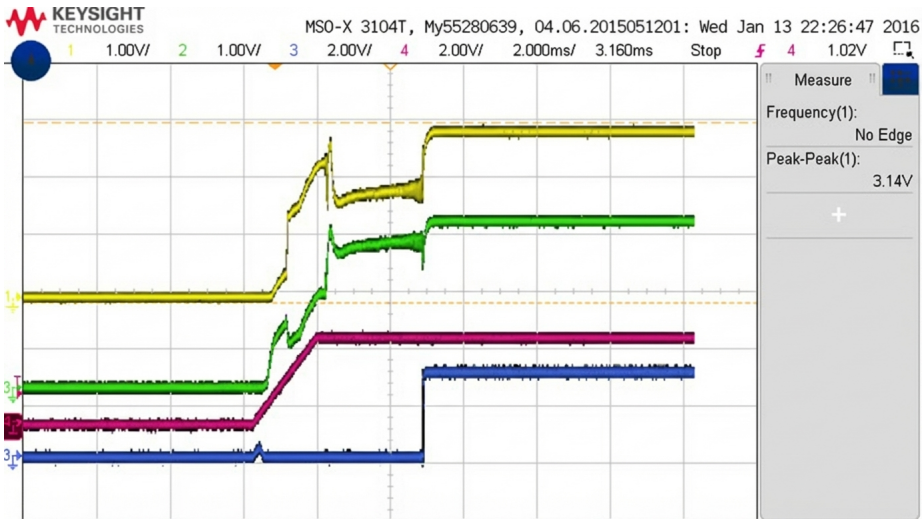

Figure 2: Figure 6

Measured phase noise at 1.5 GHz loop output frequency
Measured phase noise results

The analysis indicates that when the loop bandwidth is 100 kHz, the noise around the useful signal is relatively weak compared to other cases. Additionally, when the loop bandwidth is smaller, a "bump" phenomenon appears outside the band because the out-of-band noise is primarily high-pass VCO noise [**?**]. With wider loop bandwidth, the phase noise curve becomes smoother and exhibits a monotonically decreasing trend compared to the other two bandwidth settings, indicating better frequency stability.

3.2.2 Acquisition Time Testing

Acquisition time measurements were conducted at a loop output frequency of 1.5 GHz with loop bandwidths set to 100 kHz, 50 kHz, and 10 kHz.

The following experiments compare PLL acquisition times with fixed loop bandwidths of 100 kHz, 50 kHz, and 10 kHz. In the diagrams, yellow, green, purple, and blue represent channels 1, 2, 3, and 4, respectively. Channels 1 and 2 correspond to the PD_D and PD_U output signals, channel 3 is the trigger level ensuring acquisition time measurement starts from loop power-on, and channel 4 is the loop lock indicator, which goes high when the loop is locked.

Measured acquisition time at 1.5 GHz

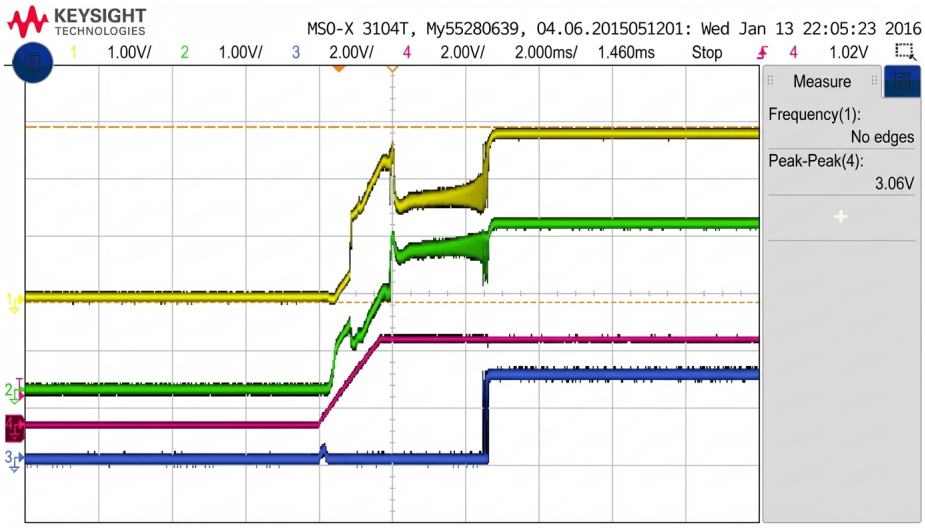

Figure 3: Figure 7

The diagrams show that the loop exhibits large transient overshoots initially after power-on due to the small damping coefficient value [**?**]. Subsequently, the differential signals at the phase detector output remain in a changing state, a phase known as frequency 牵引. After a period of frequency 牵引, the loop error voltage stabilizes near zero, indicating that the loop has locked onto the input frequency. The loop acquisition time is the duration from the initial unlocked state to the locked state.

Measured loop acquisition time results

The analysis demonstrates that under identical system parameter settings, loop bandwidth significantly affects acquisition time. Larger loop bandwidth results in shorter acquisition time and stronger acquisition performance.

3.3 Experimental Conclusions

Both simulation analysis and measurement results conclude that selecting an appropriate loop bandwidth is crucial for PLL frequency synthesizers. During loop design, both phase noise and acquisition time should be considered simultaneously to choose the optimal loop bandwidth that achieves strong acquisition performance with minimal phase noise, thereby meeting design technical specifications.

4 Conclusion

The design scheme, simulation analysis, and experimental results demonstrate that using the PE3236 chip enables miniaturized, low-power design of L-band

PLL frequency synthesizers while meeting technical specifications. This work also investigates the relationship between loop output phase noise, acquisition time, and loop bandwidth. As communication technology advances and demands for frequency synthesizer performance become more stringent, the development of high-performance PLL frequency synthesizers will have broader prospects.

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Figures

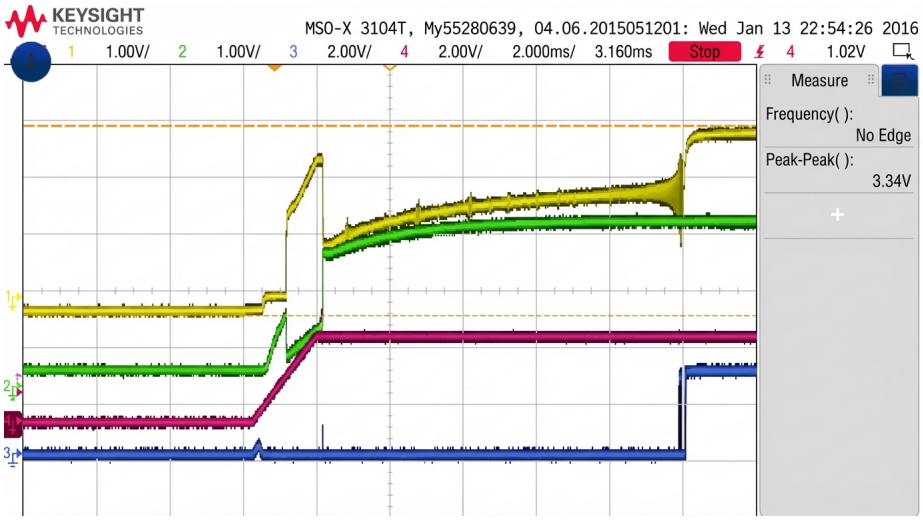

Figure 4: Figure 8