Signal Processing Implementation Analysis for FPGA-based AgileDARN Radar Digital System (Postprint)

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Abstract

This paper, based on the Agile coherent ground-based high-frequency radar (AgileDARN) system, reviews the research background of ionospheric sounding and briefly introduces the AgileDARN radar system. It analyzes the digital signal processing system, elaborates on the workflow of the system transmit signal generation module and echo signal processing module, designs the hardware architecture of the digital system, provides a detailed analysis of the mechanism for multi-pulse sequence generation of system transmit signals and the detailed steps of echo signal processing, implements the generation of raw signals, array antenna signal beamforming processing, and digital filter design in the system using FPGA, and verifies through simulation experiments the feasibility and effectiveness of the FPGA design, thereby meeting the design requirements of the AgileDARN radar digital system.

Full Text

Analysis of Signal Processing Implementation for an FPGA-Based AgileDARN Radar Digital System

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Abstract

This paper reviews the research background of space ionosphere detection based on the AgileDARN (Agile Dual Auroral Radar Network) radar system and provides a brief introduction to the system architecture. It analyzes the digital signal processing system, elaborates on the workflow of the transmit signal generation module and echo signal processing module, designs the hardware architecture, and presents a detailed analysis of the mechanism for generating multi-pulse transmission sequences and the detailed steps of echo signal processing. The paper also examines the FPGA implementation of original signal generation, array antenna signal beamforming, and digital filter design within the system. Simulation experiments verify the feasibility and effectiveness of the FPGA design, demonstrating that it meets the design requirements of the AgileDARN radar digital system.

Keywords: FPGA, AgileDARN, Array Antenna, Digital Beamforming (DBF), Digital Filter

0 Introduction

The ionosphere is a partially ionized upper atmosphere above 60 km altitude, representing the primary operational region for spacecraft and the main medium for radio wave propagation. Disturbances in the ionospheric environment can significantly impact various space platforms based on space technology. China' s vast mid- and low-latitude regions lie within the global high-incidence zone of ionospheric scintillation, where ionospheric disturbance amplitudes can exceed 15 dB, frequently causing communication interruptions and increased bit error rates. For satellite navigation, positioning errors can reach hundreds of meters, and GNSS satellites in low-latitude regions can experience short-term failures or even continuous interruptions lasting several hours due to ionospheric disturbances. Ground-based radar target detection and strategic early warning are also severely affected. Understanding ionospheric characteristics and artificially modifying the ionosphere constitute an important foundation for space information countermeasures.

The international Super Dual Auroral Radar Network (SuperDARN) was established precisely to study ionospheric anomalies in mid- and high-latitude regions. Over the past 30 years, SuperDARN has become the most important observational tool for studying polar ionospheric activities due to its extensive geographical coverage and high-precision continuous measurements. SuperDARN consists of several dozen ground-based high-frequency radars operating at 8-20 MHz, built through cooperation among more than 10 countries including the United Kingdom, United States, Australia, and Japan. China also constructed two SuperDARN high-frequency radars at the Zhongshan Station in Antarctica in 2010. Currently, SuperDARN covers the polar ionosphere and parts of the mid- and high-latitude ionosphere [1]. High-frequency radars in mid- and high-latitudes are primarily distributed in the Western Hemisphere, with only one set

deployed in the Eastern Hemisphere (Japan), which cannot satisfy SuperDARN' s requirement for large-scale coverage of global ionospheric convection patterns [2]. To fill the data gap in the Eastern Hemisphere' s mid- and high-latitudes (mainly over China), the Chinese Academy of Sciences' National Space Science Center is developing a highly flexible high-frequency radar (called AgileDARN) under the support of the 12th Five-Year 863 Program. Based on fully digital phased array radar technology, this radar can more flexibly adjust most of its detection parameters according to specific scientific research requirements.

As a member of the SuperDARN radar network, the AgileDARN radar, like other high-frequency radars, employs a dual-antenna array architecture—a 16-element main array and a 4-element interferometric sub-array. The main array is used for both signal transmission and echo reception, while the sub-array only receives echoes. While drawing on traditional SuperDARN design concepts, AgileDARN incorporates independent innovation to design and develop a high-performance radar system based on fully digital phased array technology, enabling arbitrary radar beam scanning and overcoming the limitations of fixed beams and fixed beam intervals in conventional SuperDARN radars. The AgileDARN radar primarily consists of three parts: the antenna array, transceiver modules, and digital unit. The digital unit serves as the heart of the radar system, controlling the radar' s operating status, generating various signals as required, and performing real-time processing of echo signals. Additionally, the digital unit enables real-time calibration of amplitude and phase errors among the transmitters and receivers in different channels. This paper focuses on the FPGA implementation of signal generation and echo signal processing methods in the digital unit [3,5].

1 Digital Signal Processing Design

The digital signal processing portion of the AgileDARN system primarily includes the transmit signal generation module and the echo acquisition and processing module. The transmit signal generation module generates the required transmit signals for each channel, which after filtering and amplification by the transmitter, are emitted by the antenna array for target detection. The echo acquisition and processing module performs a series of processing steps on the echo signals after AD sampling to obtain the required data.

1.1 Transmit Signal Generation Module

The transmit signal generation module is responsible for producing 16-channel transmit signals. The module primarily consists of a DA processing board and a DA playback board. The processing board receives operating parameters configured by the host computer to perform pulse modulation and main-beam DBF processing for the transmit branches, then transmits the processed data to the DA playback board, which converts the data into analog signals. The core of the transmit signal generation module is the DA processing board.

The FPGA on the DA processing board must complete several functions: configuring the DAC chip to set its operating mode and requirements for normal operation; generating original signals using internal FPGA IP cores; replicating signals into 16 channels and performing amplitude-phase consistency error correction for the transmit channels; completing beamforming and beam position switching; and implementing clock distribution and communication with the host board.

The signal processing flow is illustrated in the figure:

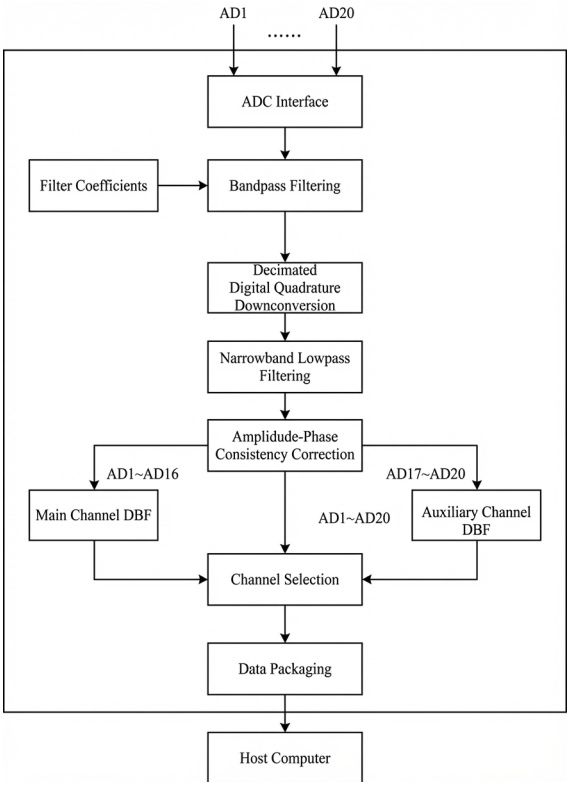

Figure 1: Figure 1

Transmit Signal Generation Flow Diagram

The FPGA transmit signal generation module employs non-uniform time-interval multi-pulse sequences to generate transmit signals, resolving the inherent contradiction between range ambiguity and Doppler velocity ambiguity in traditional SuperDARN radars. The pulse width setting improves range resolution, the minimum delay interval between pulses determines the maximum Doppler frequency shift for optimized resolution, and the length of the multi-pulse sequence improves temporal resolution. Consequently, the

FPGA software includes a system control module, a code generation module for operating modes, an amplitude-phase correction module, and a digital beamforming module. The system control module outputs clock signals, clock switching signals, trigger signals, and user debugging LED indicator signals for the other modules.

1.2 Echo Acquisition and Processing Module

The echo acquisition and processing module needs to acquire 20 channels of echo signals, including 16 main channels and 4 auxiliary channels. The collected data is processed by an FPGA processing board, which performs filtering, down-conversion, calibration, and other processing on the AD-sampled signals to obtain valid radar data.

The software design functions include: ADC chip configuration, bandpass filtering, digital quadrature down-conversion and decimation, amplitude-phase consistency error correction for 20 receive channels, beamforming, and data packaging and uploading. The signal processing flow is shown in Figure 2

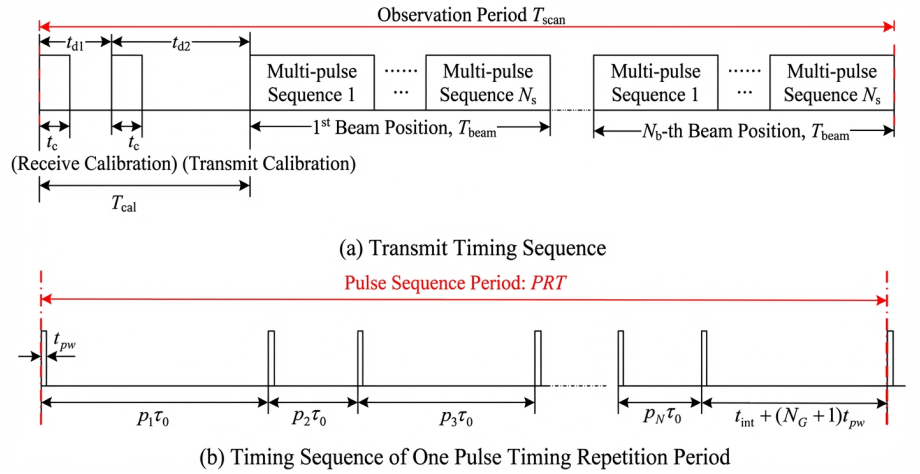

Figure 2: Figure 2

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Figure 2 Echo Acquisition and Processing Flow Diagram

The bandpass filter primarily suppresses out-of-band interference signals in the collected data. The FPGA receives the raw intermediate frequency data sampled by the ADC and performs digital quadrature down-conversion to implement orthogonal detection of the signal, outputting I and Q quadrature signals to obtain phase information. To reduce the data rate, decimation is required after quadrature down-conversion. Simultaneously, to avoid mixing interference introduced during digital down-conversion and harmonic interference caused by

signal decimation, narrowband filtering is applied to the I and Q signals separately before amplitude-phase consistency correction.

Due to hardware non-idealities, different receive channels in the entire system exhibit amplitude-phase consistency errors. The echo processing module uses calibration data to correct these amplitude-phase errors in the receive channels. The correction principle involves complex multiplication of the AD-collected 16-channel echo data with compensation factors for each channel. After correction, the transmit signals complete digital beamforming (DBF) through selection of different beam positions. The weighting factors required for beamforming operations are configured by the host computer and weighted (complex multiplied) with the echo acquisition data. The system DBF operation employs a mechanism of parallel 7-channel processing for the 16 main-channel echo signals and separate processing for the 4 auxiliary channels, enhancing the radar system' s angular resolution and detection range to enable observation of different beam directions. The processed echo data is packaged and stored for subsequent data analysis and research.

2.1.1 Operating Timing Design

When operating in normal mode, the AgileDARN radar system works with a signal frequency range of 8-20 MHz, generated by the transmit signal generation module and transmitted through the array antenna for target detection. The receiver acquires echo data, which after amplitude-phase correction and beamforming, produces the final data. The AgileDARN radar system employs a non-uniform time-interval multi-pulse sequence detection method to generate transmit signals. The transmit timing during normal operation of the generation module is shown in Figure 3 [FIGURE:3].

Figure 3 Timing Design for Three Observation Modes

In the operating timing, one observation period includes receive calibration pulses, transmit calibration pulses, and multi-pulse sequences for multiple beam positions. The pulse timing within each multi-pulse sequence is shown in Figure 3(b). Each different beam position in the timing represents a different beam direction of the array antenna, enabling arbitrary directional scanning of the antenna pattern' s main beam and overcoming the limitations of fixed beams and fixed beam intervals in traditional SuperDARN radars. The transmit signal consists of multiple observation periods, with each multi-pulse sequence containing parameters such as pulse width τ, minimum delay interval t_0, pulse count, pulse sequence length, number of data beam positions, and number of multi-pulses. These parameters are directly related to range resolution and temporal resolution.

2.1.2 FPGA Implementation of Operating Timing

To simplify the FPGA hardware logic burden, the parameters for the operating timing shown in Figure 3 are configured by the host computer. The host computer sends parameters such as operating frequency, pulse width τ, minimum delay interval t_0, number of data beam positions, number of multi-pulses, and intervals between pulses to the FPGA chip. The FPGA design logic uses trigger signals to initiate each pulse generated in the transmit signal operating timing. Based on these parameters, the FPGA parses the trigger signals for receive calibration, transmit calibration, and sub-pulse generation. By detecting the rising edge of the trigger signals, the FPGA enables the Xilinx DDS Compiler Core to generate the corresponding original transmit signals when the detection result is high. Simultaneously, the FPGA analyzes the pulse width parameters configured by the host computer to control the termination of pulse signals. The timing simulation generated by ModelSim is shown in Figure 4 [FIGURE:4].

Figure 4 Single-Channel Transmit Signal Timing Diagram

The first waveform in the figure represents the pulse trigger signal parsed by the FPGA based on the parameters sent from the host computer. The arrival of the trigger signal marks the generation of the transmit signal pulse. The FPGA counts the pulse width and stops signal generation when the width meets the required value. The third waveform shows the generated transmit signal, with the first and second pulses from the left being receive calibration and transmit calibration data, respectively, and the remainder being data sub-pulses. The FPGA test results match the designed operating timing exactly.

Each pulse is designed as a transmit signal with configurable frequency and phase. The sub-pulses in Figure 4, when magnified, appear as shown in Figure 5 [FIGURE:5]. In the Xilinx ISE programming environment, the original transmit signal is generated by the Xilinx DDS Compiler Core, which can be configured with different frequency and phase requirements through the corresponding control ports to produce the desired original signals.

2.2.1 Digital Filter Design

A digital filter is a linear time-invariant system implemented with a predetermined finite-precision algorithm that converts input digital signals into desired output digital signals. The entire AD data processing pipeline employs bandpass filters, lowpass filters for digital down-conversion, and narrowband lowpass filters. The radar' s digital system designs digital filters using FIR filter IP cores in the FPGA.

The FDATool in MATLAB is used to set parameters for the bandpass and lowpass filters and select the coefficient quantization bit width. After completing the design parameter settings, the tool can directly generate coefficient configuration files (COE files) required by the FPGA. These are imported directly into the FIR filter IP core via the FPGA to generate the corresponding digital

filters.

Due to the different center frequencies of the radar system' s transmit calibration data, receive calibration data, and echo data, two sets of digital filters are needed for real-time processing of sampled data after AD conversion. The receive calibration data and echo data have a sampled center frequency of 10 MHz, while the transmit calibration data has a sampled center frequency of 8-20 MHz. Figure 5 shows the amplitude-frequency response curve of one of the bandpass filters required by the system, with a center frequency of 10 MHz, passband of 2 MHz, and quantization bit width of 16 bits.

Figure 5 Amplitude-Frequency Response Curve of Bandpass Filter

Due to FPGA chip resource constraints, the two filter sets share a single filter IP core resource. During real-time filtering processing, a time-division multiplexing mechanism is employed, requiring filter switching based on data requirements. In FPGA implementation, the two sets of bandpass filter coefficient files are loaded into the FIR filter IP core through its two channels. The FPGA generates switching signals based on the different center frequencies of the received signals and configures different filter instructions for the IP core through configuration ports to switch filter coefficients for different data. The configuration port instructions are shown in Table 1 .

Filter Coefficients	First Channel Filter	Second Channel Filter	Configuration Port Instruction
8' b00000000	8' b00000001		

Table 1 FIR Filter Coefficient Configuration Instructions in FPGA

The lowpass and narrowband lowpass filters are digital filters with decimation characteristics. In FPGA design, FIR filter IP cores are used by configuring the decimation parameters. To save multiplier resources, registers can also be defined to count data and perform controllable decimated filter data output when the decimation parameters are met.

By meeting the filter design parameters shown in Figure 5, the digital bandpass filter is designed through FPGA and the corresponding parameters are configured. MATLAB is used to simulate raw data, which is input into the FPGA filter, and the output data is used to plot the amplitude-frequency response curve shown in Figure 6

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Figure 6 Up. Input simulated raw signal spectral response; Down. Filter output signal spectral response. The abscissa is frequency (MHz), the ordinate is amplitude response (dB)

The figure shows that the filtering results are consistent with the designed filter response curve. Compared with the original data above, out-of-band signals are

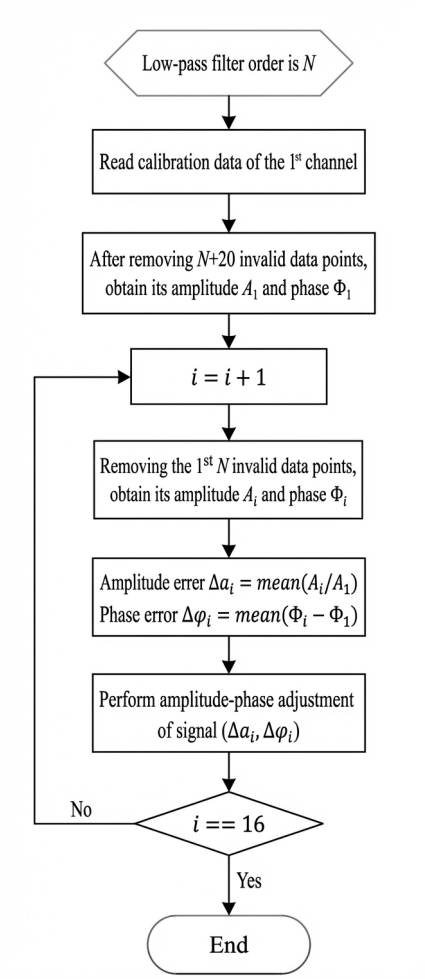

Figure 3: Figure 6

filtered out. The filtering performance of other bandpass and lowpass filters was verified through simulation experiments. Therefore, the simulation results demonstrate that the FIR filter implemented based on IP cores functions correctly and meets design requirements. Due to its flexibility, the FIR filter implemented via IP cores can select appropriate hardware resource amounts and data processing speeds based on parameter settings, making it a major focus for future digital filter applications.

2.2.2 Amplitude-Phase Consistency Correction Implementation

The AgileDARN radar system consists of 16 transmit channels and 20 receive channels. Due to hardware non-idealities, amplitude-phase inconsistencies exist between channels. To reduce the impact of channel inconsistencies, calibration data is used to correct amplitude-phase errors in transmit and receive signals for each channel. AgileDARN radar employs internal calibration with a period consistent with the pulse sequence period. Internal calibration is performed during the gap between the end of the first pulse transmission and the arrival of the first echo in each pulse sequence period, including transmit chain calibration and receive calibration chain. During calibration, the calibration signal provided by the signal generation module is $s_0(t)$, and the signal obtained after passing through the chain is $s_{RT}(t)$. The relationship between them is:

$$s_{RT}(t) = a_{RT} e^{-j\phi_{RT}} s_0(t)$$

where $s_0(t)$ is known and $s_{RT}(t)$ can be measured. Based on this equation, the amplitude-phase characteristics of the transmit-receive channel can be obtained for calibrating consistency across channels.

Figure 7 [FIGURE:7] Acquisition of Compensation Factor

During amplitude-phase consistency correction, the host computer needs to configure compensation factors for each channel. After obtaining calibration data from Channel 1, the host computer eliminates invalid data and calculates the channel amplitude A_1 and phase Φ_1 through expression (1). The same method is used to obtain amplitudes and phases for all subsequent channels. Using Channel 1 output as a reference, amplitude errors Δa and phase errors $\Delta\phi$ for each channel are calculated. The method for obtaining compensation factors is shown in Figure 7. The host computer configures and sends compensation factors to the FPGA IP core for storage. For different beam position data, the FPGA configures the corresponding compensation factors to be complex-multiplied with the I/Q signals in the channel based on the beam selection signal sent from the host computer, producing compensated and corrected I/Q signals. The operating principle is shown in Figure 8 [FIGURE:8].

Figure 8 Principle of Amplitude and Phase Consistency Correction

The digital system designs the amplitude-phase consistency processing using IP cores within the Xilinx FPGA. The host computer communicates with the FPGA chip to send compensation factors via the AXI-streaming protocol bus, storing them in the RAM Core within the chip. To enable multi-beam position scanning, the system generates beam switching signals based on different beam positions. The FPGA reads different compensation factors corresponding to different beam positions from the RAM Core based on these signals and uses the integrated Complex Multiplier Core within the FPGA to perform AXI protocol-format complex multiplication of the original signals and compensation factors when its enable port is active, generating corrected transmit signals.

2.2.3 DBF Implementation in FPGA

The AgileDARN radar is a phased array radar with flexible beam pointing that can simultaneously form multiple independent beams for full-direction scanning. The entire radar system employs array antennas with two arrays—a main transmit-receive array and an interferometric sub-array—with each antenna corresponding to one transceiver channel. During signal processing, data must be beamformed through phase shifting and weighting.

Assuming the quadrature baseband signals for channel k are I_k and Q_k, and the beam direction is θ_B, the intra-array phase compensation is:

$$\Delta\phi_B = \frac{2\pi d}{\lambda}\sin\theta_B$$

Each channel' s transmit signal achieves transmit antenna pattern synthesis and different beam scanning through phase shifting and weighting of the original signal. The phase shift weighted processing for a single channel is shown in Figure 9 [FIGURE:9].

Figure 9 Single-Channel Phase Shift Weighted Processing (DBF)

The formula for the beamformed output signal is:

$$\begin{bmatrix} I'_k \\ Q'_k \end{bmatrix} = \begin{bmatrix} \cos\Delta\phi_B & -\sin\Delta\phi_B \\ \sin\Delta\phi_B & \cos\Delta\phi_B \end{bmatrix} \begin{bmatrix} I_k \\ Q_k \end{bmatrix}$$

Thus obtaining beamformed data $z_k = I'_k + jQ'_k$.

To meet the requirement of observing one main lobe and three side lobes on each side, the AD sampling processing module needs to perform parallel 7-channel DBF processing on the 16 main-channel received signals, with the 7 beam positions cycling according to the user-configured beam sequence, while the 4 auxiliary receive signals undergo single-channel processing. Taking the main channel as an example, the processing structure for the 7 parallel DBF channels is shown in Figure 8 [FIGURE:8].

Figure 8 DBF of Parallel 7 Channels

After receiving the corrected 16 main-channel data, the FPGA replicates each channel into 7 copies, totaling 112 data streams. The host computer configures and stores weighting factors for each channel via the AXI-streaming protocol in the FPGA' s RAM Core. Based on different beam position signals, the FPGA reads different weighting factors from the RAM Core and performs AXI protocol-format complex multiplication of the original signals and phase shift factors to complete beamforming operations. The DA processing board can directly use the Complex Multiplier Core to complete beamforming operations. For the AD processing board, due to limited multiplier resources in the chip, beamforming cannot use the Complex Multiplier Core. Instead, the FPGA must invoke multipliers and employ time-division multiplexing, using one multiplier to implement one beamforming operation by time-multiplexing the multiplication of the real and imaginary parts of the corrected sampled data and weighting factors, thereby reducing the number of multipliers used.

3 Conclusion

Currently, the hardware development and corresponding FPGA program design for this system have been completed, and the functions of each module in the digital system have been basically realized. Through detailed analysis of the technical requirements for the AgileDARN radar digital processing system, FPGA implementation of transmit signal generation, debugging, and output has been achieved. Additionally, functions required for echo signal processing —including bandpass filtering, digital down-conversion, lowpass filtering, and beamforming—have been designed and simulated, meeting the technical requirements of the AgileDARN radar system. Design and experimental analysis of this system demonstrate that FPGA circuits offer strong flexibility and operability for digital signal processing, along with high reliability. This facilitates arbitrary scanning of AgileDARN radar beams, overcoming the limitations of fixed beams and fixed beam intervals in traditional SuperDARN radars, while enabling observation of the main beam echo signal and three side lobe echoes on each side, thereby achieving flexible scanning of ground-based high-frequency radar beams and observation over a large spatial field of view.

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