FPGA Implementation of Digital Signal Processing for AgileDARN Radar (Postprint)

Authors: Song Jiang, Lan Ailan, Yan Jingye, Sun Lin

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Abstract

The AgileDARN radar system is a high-sensitivity ground-based high-frequency radar system based on fully digital phased-array technology for ionospheric detection at mid-to-high latitudes. This paper investigates the digital signal processing of the radar system, designs and analyzes the transmit/receive signal processing flow, and implements signal transmission and reception, amplitude-phase inconsistency correction, digital filtering, and digital beamforming processing on FPGA chips, thereby enabling flexible scanning of the radiation pattern and improved direction-finding accuracy. Simulation results verify the feasibility and effectiveness of the FPGA design.

Full Text

Preamble

FPGA Implementation of Digital Signal Processing for AgileDARN Radar

Song Jiang[1],[2], Ailan Lan[1], Jingye Yan[1], Lin Sun[3]
[1](Key Laboratory of Microwave Remote Sensing, National Space Science Center, Chinese Academy of Sciences, Beijing, 100190, China)
[2](University of Chinese Academy of Sciences, Beijing, 100049, China)
[3](School of Information and Electronics, Beijing Institute of Technology, Beijing, 100081, China)

Abstract

The AgileDARN radar system is a sensitive ground-based coherent high-frequency radar based on all-digital phased array technology for detecting the ionosphere at middle and high latitudes. This paper investigates the digital signal processing of the radar system, designing and analyzing the transmit and receive signal processing flow of the radar' s digital system. Based on FPGA chips, we implement signal transmission and reception, amplitude-phase inconsistency correction, digital filtering, and digital beamforming processing, enabling flexible scanning of radiation patterns and improved echo direction accuracy. Simulation experiments verify the feasibility and effectiveness of the FPGA design.

Keywords: FPGA, AgileDARN, SuperDARN, Array Antenna, Digital Beamforming (DBF), Digital Filter

1 Introduction

The ionosphere is the ionized upper atmosphere above 60 km, representing the primary operational region for spacecraft and the main medium for radio wave propagation. Disturbances in the ionospheric environment significantly impact space platforms based on space technology, with ionospheric perturbation amplitudes exceeding 15 dB, frequently causing communication interruptions and increased bit error rates. These disturbances can introduce positioning errors up to hundreds of meters for satellite navigation and severely affect target detection and strategic early warning capabilities of ground-based radars. Consequently, understanding ionospheric characteristics and artificially modifying the ionosphere has become critically important [1,2].

The International Super Dual Auroral Radar Network (SuperDARN) was established to study ionospheric anomalies at middle and high latitudes. Due to its extensive geographic coverage and high-precision continuous measurements, SuperDARN has gradually become an essential observational tool for studying polar ionospheric activities [3]. The network consists of several dozen ground-based high-frequency radars operating at 8-20 MHz, built through collaboration among more than ten countries including the United Kingdom, United States, Australia, and Japan [4]. China constructed a SuperDARN high-frequency radar at Zhongshan Station in Antarctica in 2010. Currently, the National Space Science Center of the Chinese Academy of Sciences is independently developing a highly flexible high-frequency radar (named AgileDARN) located in Jiamusi City, Heilongjiang Province, which will be used to probe the ionosphere over China's middle and high latitude regions, filling the data gap of the SuperDARN radar network over Chinese territory.

Drawing on traditional SuperDARN design concepts, the AgileDARN radar employs a dual-array detection scheme: a 16-element main array with transmit-receive capability and a 4-element sub-array with receive-only capability. As a new-generation SuperDARN radar, AgileDARN utilizes all-digital phased array technology, enabling arbitrary radar beam scanning and overcoming the limitations of fixed beams and fixed beam intervals in conventional SuperDARN radars. The AgileDARN radar primarily consists of three components: the antenna array, transceiver modules, and the digital system [5,6]. The digital system serves as the heart of the radar, implementing radar operating state control, transmit signal generation, and real-time echo signal processing. This paper focuses on the FPGA implementation of signal generation and echo signal processing in the digital system.

2 Radar Digital System

The digital signal processing portion of the AgileDARN system primarily includes a transmit signal generation module and an echo acquisition and processing module. The transmit signal generation module produces the required transmit signals for each channel, while the echo acquisition and processing module performs a series of preprocessing steps on the echo signals after AD sampling to obtain the desired data.

The AgileDARN radar employs a "16+4" dual-array configuration, comprising a 16-element transmit-receive main array and a 4-element receive-only sub-array, resulting in 16 transmit channels and 20 receive channels.

2.1 Transmit Signal Generation Module

The transmit signal generation module needs to produce 16 channels of transmit signals and consists mainly of a DA processing board and a DA playback board. The processing board receives operating parameters configured by the host computer to generate transmit signals, while the DA playback board converts the data into analog transmit signals.

The FPGA on the DA processing board must complete several functions: (1) configure the DAC chip to ensure normal operation; (2) generate signals; (3) modulate into 16-channel signals and perform transmit channel inconsistency correction for each; and (4) apply phase weighting to transmit signals according to beam steering requirements. The main processing flow of the transmit signal generation module is shown in [Figure 1: see original paper].

2.2 Echo Acquisition and Processing Module

The echo acquisition and processing module needs to acquire 20 channels of echo signals, including 16 main channels and 4 auxiliary channels. The acquired data undergoes preprocessing such as filtering and down-conversion on the FPGA processing board to obtain valid radar echo data. The signal processing flow is illustrated in [Figure 2: see original paper].

In this module, the bandpass filter primarily suppresses out-of-band interference signals in the acquired data. The FPGA receives raw intermediate frequency data sampled by the ADC, performs digital quadrature down-conversion, and outputs I and Q orthogonal signals to obtain phase information. To reduce the data rate, decimation is applied to the data after quadrature down-conversion. Additionally, to avoid mixing interference introduced during digital down-conversion and harmonic interference caused by signal decimation, narrowband filtering is applied to the I and Q signals separately before amplitude-phase inconsistency correction. Due to hardware non-idealities across the system, amplitude-phase inconsistency errors exist between different receive channels. The echo processing module uses calibration data to correct these amplitude-phase errors in the receive channels. Through different beam position selections, digital beamforming (DBF) is completed on the corrected receive signals. The system DBF operation employs a mechanism of parallel 7-beam processing for the 16 main channel echo signals and single-beam processing for the 4 auxiliary channels, improving the radar system' s angular resolution and detection range to complete detection for different beam directions.

3.1 Transmit Timing Design

The maximum detection range of SuperDARN radar exceeds 3000 km, while ionospheric drift velocities at middle and high latitudes can reach up to 2000 m/s. To resolve the conflict between range ambiguity and velocity ambiguity, non-uniform time-interval multi-pulse sequences are employed for detection [8]. Additionally, to reduce the impact of inter-channel inconsistencies in the radar, the transmitter and receiver are calibrated at the beginning of each observation period. The specific transmit timing is shown in [Figure 3: see original paper]. Each period' s timing is divided into calibration and target detection portions. Calibration includes receive calibration and transmit calibration, while target detection involves observation of various beam positions within the radar' s field of view. Calibration uses single-pulse sequences, whereas target detection employs multi-pulse sequences, with the multi-pulse sequence format remaining consistent within the same observation period.

The transmit timing shown in the figure contains multiple adjustable parameters, including pulse width, minimum delay interval, and various pulse intervals. These parameter settings directly relate to radar performance metrics such as detection range, range resolution, and time resolution [7,8]. An observation period includes receive calibration, transmit calibration, and N multi-pulse sequences, as shown in Figure 3: see original paper. The N multi-pulse sequences used for target detection characterize N different beam directions and dwell times. Figure 3: see original paper illustrates the target detection pulses.

To simplify the FPGA hardware resource burden, the various parameters in the operating timing are configured by the host computer. The FPGA design logic operates as follows: each pulse in the operating timing is initiated by a trigger signal. The FPGA parses the trigger signals for receive calibration, transmit calibration, and target detection sub-pulses, and uses the DDS Compiler Core to generate the corresponding original transmit signals upon detecting the rising edge of the trigger signal. Simultaneously, the FPGA receives parameters such as pulse width configured by the host computer to control pulse signal termination. As shown in Figure 4: see original paper, a timing simulation diagram generated through ModelSim [9] demonstrates this process. The first waveform in Figure 4: see original paper shows the pulse trigger signal parsed by the FPGA, whose arrival marks the generation of the transmit signal pulse.

The FPGA counts the pulse width and stops signal generation when the width meets the required value. The third waveform shows the generated transmit signal, where the first and second pulses from the left are receive and transmit calibration data, respectively, with the remainder being target detection sub-pulses. The FPGA test results shown in Figure 4: see original paper match the designed operating timing exactly.

3.2 Digital Filter Design

After AD sampling and digital down-conversion, signals experience harmonic interference, intermodulation interference, and cross-modulation interference. To reduce these effects and improve signal-to-noise ratio, digital bandpass filtering is required after AD sampling to remove interference introduced during sampling. Additionally, low-pass filtering is needed after digital down-conversion to eliminate the sum-frequency components introduced by digital quadrature mixing. To further suppress out-of-band interference, narrowband low-pass filtering is applied. These filters are designed based on the FIR filter IP core in FPGA [12].

Before FPGA implementation, the coefficient configuration files (COE files) for the digital filters must be generated using the FDAtool in MATLAB. These coefficient files are then imported into the FPGA FIR filter IP core to generate the digital filters [9,10].

3.2.1 Bandpass Filter

The receive calibration data and echo data in the echo sampling module have a frequency of 70 MHz. After 60 MHz sampling, the center frequency becomes 10 MHz, while the transmit calibration data has a center frequency of 8–20 MHz after sampling. Therefore, two sets of bandpass filters are needed for real-time processing of sampled data after AD sampling. [Figure 5: see original paper] shows the amplitude-frequency response curve of one required bandpass filter, with a center frequency of 10 MHz and a passband of 2 MHz.

Due to DSP resource limitations in the FPGA chip, the two filter sets share a single filter IP core resource. During real-time filtering processing, a time-division multiplexing mechanism is employed, requiring filter switching based on sampling data. In FPGA implementation, the two sets of bandpass filter coefficient files are loaded into the FIR filter IP core through its two channels. The FPGA generates switching signals based on the different center frequencies of received signals and issues commands through the IP core configuration port to switch filter coefficients in real time. The configuration commands are shown in [11].

By configuring the design parameters of the filter in [Figure 5: see original paper] through FPGA to generate the digital bandpass filter and using MATLAB to simulate raw data, the amplitude-frequency response curve after filtering is shown in [Figure 6: see original paper]. Comparison reveals that out-of-band signals are effectively filtered out.

3.2.2 Low-Pass Filter

The AD data acquisition process involves two stages of low-pass filtering: low-pass filtering after quadrature down-conversion and narrowband low-pass filtering. The low-pass filter in digital quadrature down-conversion removes sum-frequency components introduced by mixing, while the subsequent narrowband low-pass filter further suppresses out-of-band interference.

To reduce system data volume and DSP resource usage, the low-pass filters after quadrature down-conversion and the narrowband low-pass filters are decimating digital filters. The system decimates the data after low-pass filtering in quadrature down-conversion by 60 times, reducing the sampling rate from 60 MHz to 1 MHz. When setting the decimation factor in the FPGA filter IP core, the relationship between decimation factor and DSP resource usage is shown in .

In FPGA design, the decimation parameter for the post-down-conversion FIR filter is configured as 6 times, while a counting decimation method is used for an additional 10 times decimation of the filtered output data, thereby achieving the 60 times decimation factor. This also reduces the data sampling rate and volume, alleviating the burden on the entire system.

Simulation experiments on bandpass and low-pass filters verify the filtering effectiveness. The FIR filters implemented based on FPGA IP cores offer flexible control and high reliability, allowing selection of appropriate hardware resources and data processing speeds through parameter configuration, making them a promising approach for future digital filter applications.

3.3 Amplitude-Phase Inconsistency Correction Implementation

The AgileDARN radar system comprises 16 transmit channels and 20 receive channels. Due to hardware non-idealities, amplitude-phase inconsistency errors exist between channels. To reduce these effects, the transmitter and receiver channels are calibrated at the beginning of each observation period to obtain amplitude and phase errors between channels. These errors are compensated in the echo acquisition processing module and transmit signal generation module to achieve channel inconsistency correction. The calibration signal generation and error compensation are implemented using FPGA, while the acquisition of amplitude-phase errors for correction is completed in the host computer. The processing method for receive channel inconsistency correction is essentially the same as for transmit channels and will not be distinguished here.

After obtaining the inconsistency errors for each channel, the host computer sends the amplitude-phase error correction factors to the digital system. Receive channel correction factors are sent to the echo acquisition processing module and applied before digital beamforming, while transmit channel correction factors are sent to the transmit signal generation module and applied before transmit beamforming. This processing is entirely completed by FPGA. The specific implementation involves the host computer transmitting inconsistency errors to the FPGA' s RAM core via the AXI-streaming protocol for storage. During operation, the FPGA' s Complex Multiplier Core performs complex multiplication in AXI protocol format between the inconsistency errors and signal data, as illustrated in [Figure 8: see original paper].

3.4 Beamforming Implementation

Digital beamforming technology is one of the most widely adopted techniques in phased array radar, offering advantages including rapid adaptive beam nulling, super-resolution direction finding, ultra-low sidelobes, beam correction for element failures, dense multi-beam formation, adaptive space-time processing, and flexible timing control. It is an essential technology for modern array signal systems [13].

The AgileDARN radar antenna array consists of two linear arrays: a 16-element main array for azimuth scanning and a 4-element receive sub-array for obtaining echo elevation information through interferometric processing with main array signals. To improve angular resolution in azimuth while maintaining temporal resolution, the AgileDARN radar employs multi-beam synthesis—specifically 7-beam synthesis—for main array echo signals. This subdivides a single beam width into seven portions (as shown in [Figure 9: see original paper]), enabling parallel beamforming of 16-channel echo signals in seven directions. By comparing the synthesis results, the azimuth direction of echoes can be determined more accurately.

The processing structure for parallel 7-beam DBF on signals from each channel is shown in [Figure 10: see original paper]. After amplitude-phase inconsistency correction, the FPGA replicates each of the 16 main channel data streams into seven copies. The host computer generates corresponding phase shift factors for the seven directions and transmits these shift factors to the FPGA' s RAM Core via the AXI-streaming protocol. Based on beam position signals, the FPGA reads different beamforming factors from the RAM Core and performs complex multiplication in AXI protocol format between the original signals and synthesis factors to complete beamforming.

The transmit signal generation module can directly use the Complex Multiplier Core for beamforming. However, for the AD processing board, due to limited DSP resources, beamforming cannot use the Complex Multiplier Core. Instead, it employs time-division multiplexing by calling multipliers to sequentially complete real and imaginary multiplications for complex multiplication, finally obtaining DBF results through superposition. This halves the number of multiplier resources by time-multiplexing the multiplication of real and imaginary parts of corrected sampling data and beamforming factors.

Due to the conflict between chip resources and functional complexity, time-division multiplexing is employed for the bandpass filter and beamforming in the echo signal acquisition module, while decimation (downsampling) is applied to other filter types. This reduces not only DSP resource usage but also overall system data volume, easing data storage burdens. shows the resource usage for implementing the bandpass filter using time-division multiplexing, compared with the DSP resources required without this approach.

4 Conclusion

This paper implements various functions of the AgileDARN radar digital system using FPGA digital circuits and Verilog HDL. Through IP cores and software logic, transmit timing generation, transmit channel inconsistency correction, and phase weighting are completed, converting transmit signals into analog form. Simultaneously, IP cores are utilized to process sampled echo signals, including bandpass filtering, digital down-conversion, low-pass filtering, receive channel inconsistency correction, and beamforming.

Bandpass and low-pass filters suppress interference introduced during sampling and down-conversion processes. Channel inconsistency correction eliminates amplitude and phase errors caused by inter-channel inconsistencies, improving radar measurement accuracy. Multi-beam synthesis of main array echoes significantly enhances angular resolution in azimuth.

The AgileDARN radar comprises 16 transmit links and 20 receive links, representing high system complexity. Higher complexity demands greater hardware resources. To conserve hardware resources and reduce costs, time-division multiplexing is employed in designing functional modules such as bandpass filtering and beamforming, saving substantial DSP resources. Using IP cores in FPGA chips enables more flexible and reliable implementation of system functions. Experimental analysis demonstrates that FPGA circuits offer strong flexibility, operability, and high reliability for digital signal processing applications.

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