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Postprint: Advances in 3D IC Testing Technology

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Abstract

This paper analyzes and introduces the latest advances in three-dimensional chip testing. It first introduces three-dimensional chip design technology, and through an analysis of this technology, examines the major challenges currently faced: novel through-silicon via (TSV) faults, incomplete circuit testing problems, pre-bond and post-bond test co-optimization issues, among others. The paper further analyzes various methods that have been proposed internationally and forecasts several future research directions.

Full Text

Abstract

This paper analyzes the primary challenges currently facing three-dimensional integrated circuit testing, including novel through-silicon via (TSV) faults, incomplete circuit testing issues, and co-optimization of pre- and post-bond testing. We examine various methods proposed internationally and identify future research directions.

Keywords: three-dimensional chips, wafer, through-silicon via, scan chain, test access mechanism

1 Introduction

Three-dimensional integrated circuit (3D IC) design has emerged as one of the fastest-growing technologies in the semiconductor industry by enabling vertical integration and dramatically increasing chip density. It is regarded as a promising approach to sustain Moore' s Law, with some experts even considering it a "beyond-Moore" design paradigm [?]. Unlike conventional planar design methodologies, 3D ICs achieve vertical integration by stacking multiple dies and interconnecting them through Through-Silicon Vias (TSVs).

This vertical integration offers numerous advantages, including reduced form factor, increased packaging density, improved bandwidth, enhanced RF and

power performance, and lower costs [?][?][?]. Recognizing the significance of 3D IC design for the integrated circuit industry, numerous research groups, particularly in the United States, have been actively investigating this area since 2004. Major corporations such as Intel and IBM have already launched corresponding process lines, substantially advancing the industrialization of 3D chips. At the national level, multiple European and American countries have initiated government-funded projects to support 3D IC research. In China, several academic institutions have also begun focusing on this field in recent years with support from national key programs and the National Natural Science Foundation.

A key distinction between 3D ICs and traditional System-on-Package (SOP) approaches is the replacement of wire bonding and flip-chip interconnects with TSVs. TSV diameters typically measure several microns [?], representing tens to hundreds of times the size of internal interconnects, thereby enabling inter-die signal connections. The number of interconnections between two dies can expand from a few thousand in SOP to between 100,000 and 1 million. Additionally, TSVs significantly reduce wiring distance between dies, with vertical heights generally ranging from 10 m to 100 m [?]—far shorter than conventional wire bonding distances. This enables high-speed inter-die signal transmission and facilitates more reliable multi-die chips, overcoming the limitations of existing packaging systems and establishing TSV technology as a highly promising innovation.

The manufacturing process of packaging multiple dies together is referred to as "bonding." [Figure 1: see original paper] illustrates an example of 3D integration. Two dies fabricated using different processes are interconnected through numerous short, die-to-die TSVs, which are partially filled with copper or completely filled with polysilicon or tungsten. Different relative orientations are possible when connecting two dies using TSVs. Figure 1(a) shows a face-to-face configuration where the metal layers of both dies are adjacent and interconnected through TSVs. This approach enables very high TSV density. For stacks exceeding two dies, face-to-back or back-to-back configurations become inevitable (Figures 1(b) and 1(c)).

When designing in a top-down manner (though the same issues apply to bottom-up design), the chip is treated as a functional whole, requiring careful partitioning of functions and circuits across different layers during single-die design. Three partitioning approaches exist based on granularity: process partitioning, architectural partitioning, and circuit partitioning. In process partitioning, each die layer is manufactured using different processes—for example, high-speed CMOS for logic circuits, high-density processes for DRAM, and specialized processes for RF circuits. These functionally distinct layers are then interconnected via TSVs. Architectural partitioning distributes different functional modules across dies based on their complete functions, with modules on each die connected through TSVs. Circuit partitioning assigns different circuits to different dies based solely on circuit topology without considering functional complete-

ness. Among these, process partitioning is the simplest to implement, while circuit partitioning offers the finest granularity and most significant performance optimization.

Currently, research in 3D IC design has primarily focused on architecture [?] and electronic design automation (EDA) [?], with relatively little attention given to testing. Some 3D design experts have even identified testing as the "foremost challenge" for 3D ICs [?]. Testing effectiveness is measured by two key factors: test quality and test cost. The drive to improve test quality stems from the need for accurate fault modeling to guide design and manufacturing optimization, while test cost depends on Design for Testability (DFT) overhead and testing time.

In the 3D IC design flow, manufacturers first fabricate individual dies and then bond multiple dies into a fully functional chip. This raises a critical question: should each die layer undergo pre-bond testing? This decision must balance the cost of single-die testing against packaging yield. The yield of multi-die stacks decreases with the number of layers, and without pre-bond testing, a single defective die would cause the entire chip to fail. The current consensus is that pre-bond testing is necessary to eliminate defective dies before bonding, and the testing methods discussed in this paper are based on this assumption.

For designs employing circuit partitioning, pre-bond testing faces a fundamental challenge: how to test circuits that may be structurally or functionally incomplete? Reference [?] proposes a design methodology for this problem, but it is not a comprehensive solution in terms of area overhead or test time, offering only a principled approach. Another significant challenge is ensuring co-optimization between pre-bond and post-bond testing environments, which differ substantially. Furthermore, 3D ICs exhibit distinct characteristics compared to 2D chips, such as heightened temperature sensitivity, necessitating greater attention to power and thermal effects during testing.

Although Chinese researchers have begun investigating 3D IC placement and routing in recent years, work on 3D IC testing remains limited. With relatively few international research results available, this area is likely to become the next major focus in the testing community. As 3D ICs may evolve into a mainstream design methodology, testing approaches will be critically important. This paper discusses key issues in 3D IC testing and introduces significant design methods and innovative solutions. Given the scarcity of research in this field, we emphasize analyzing pressing problems that require deeper investigation, hoping to inspire domestic testing researchers and accelerate progress in 3D IC testing.

2 Testing of 3D Integrated Circuits

Pre-bond testing is crucial and is typically performed at the wafer level using probes. The wafer is fixed on a probe card, and probes contact the die's internal pads to apply or receive signals for testing. To ensure proper contact, probes must apply significant pressure (3-10g per probe), which can total 60-120kg for

dies with numerous pads. This pressure is problematic for 3D ICs with thin substrates, necessitating new methods to compress I/O port counts or develop non-contact testing techniques.

The most significant difference between 3D and 2D IC testing is the introduction of TSVs and ultra-thin substrates. Multiple dies are connected through TSVs that must be precisely aligned; misalignment can introduce excessive delay and cause timing faults. Additionally, ultra-thin substrates increase the probability of open-circuit faults, requiring careful attention to these failure mechanisms.

Test cost must be considered when selecting 3D IC design methodologies. From a commercial perspective, the key criterion is the method' s contribution to total lifecycle cost, with chip yield being a critical factor. Pre-bond testing incurs costs but ensures higher post-bond yield. Since any die failure causes the entire chip to fail, the probability of failure becomes very high for multi-die stacks without pre-bond testing. Therefore, the decision to perform pre-bond testing must weigh its cost against yield degradation. This analysis requires a comprehensive lifecycle test cost model that examines relationships between yield, process parameters, and design scale while considering DFT overheads such as area, power, and performance penalties to enable holistic evaluation of 3D IC testability designs and methods.

While TSV failure mechanisms involve novel fault models and test generation, these topics are beyond this paper's scope due to length constraints. Instead, we focus on higher-level issues introduced by 3D design, such as testing incomplete circuits resulting from partitioning and co-optimization challenges.

3 Testing Issues and Solutions for Incomplete Circuits

A significant distinction between 3D IC testing and traditional SOP or multi-module system testing is that individual dies in a 3D stack may be functionally or structurally incomplete, presenting new testing challenges.

3.1 Testing Methods for Incomplete Logic Circuits

Designing test structures for each die layer must address two aspects: (1) ensuring adequate fault coverage for each layer' s logic circuits while minimizing test cost, and (2) enabling upward scalability so that the structure remains usable when multiple layers are integrated. One approach adapts the "test island" architecture from the Alpha processor [**?**]. As shown in [Figure 3: see original paper], each layer incorporates a "Layer Test Controller" that provides interfaces to adjacent layers, enabling integration of all layers in a chip that can ultimately connect to test equipment through a JTAG (IEEE 1149.1 standard) interface.

For each die layer, circuit inputs may originate from external interfaces or from inter-layer connections through TSVs driven by signals from other dies. These two input types require different testing approaches. For TSV-connected inputs, scan cells can be inserted and chained together to control these interfaces via

scan shifting, thereby reducing the number of probe contacts. This creates two driving sources for TSV-connected inputs: the normal operational source through TSVs and the test source through scan cells. To separate these sources for different applications, the design shown in [Figure 4: see original paper] can be used. A pass gate inserted between the scan cell and TSV is controlled by a test enable signal. During pre-bond testing, the test enable signal activates the pass gate, allowing the scan cell to drive the signal (the TSV connection remains high-impedance at this stage). During post-bond operation, the test enable signal is deactivated, the pass gate turns off and presents high impedance, and the input is driven exclusively by signals from the TSV.

As illustrated, each TSV requires a corresponding scan cell and pass gate. Since 3D IC designs incorporate numerous TSVs, this approach introduces significant area overhead and design complexity. Optimization is needed to reduce the number of required scan cells and pass gates through careful architectural design.

3.2 Testing Methods for Incomplete Clock and Power Networks

In 3D IC designs, functional modules' clock networks may be distributed across different die layers from their logic circuits. In the complete 3D stack, clock networks connect to their driven logic circuits through TSVs, but they remain separate before bonding. Without clock driving signal paths, sequential elements cannot function, preventing scan testing that relies on multiple scan cells (sequential elements) working in concert.

The same issue affects power networks. If a single die' s power distribution network is incomplete, the power system cannot drive the die to complete pre-bond testing.

One solution involves designing complete clock networks on each die through redundant design to provide test clocks for pre-bond testing. However, the primary drawback of redundant clock networks on individual dies is the difficulty they introduce for placement and routing. While 3D packaging enables complete clock networks through multi-die cooperation, implementing complete but redundant clock networks on each die separately creates post-bond redundancy, increasing design effort and imposing new constraints that limit optimization effectiveness. Even with redundant clock and power networks, balancing pre- and post-bond designs remains challenging. Pre- and post-bond test clocks must maintain zero skew, but they are not identical for a given die. The same point may need to connect to different sub-clock networks before and after bonding with different loads, requiring careful design and novel algorithms and circuit structures to achieve zero skew.

4 Co-Optimization of Pre- and Post-Bond Testing

The 3D IC testing flow comprises two steps: pre-bond testing and post-integration testing, making total test cost the sum of both components. From a

total cost perspective, test structure and method optimization must minimize overall test cost, necessitating co-optimization of pre- and post-bond testing.

From a scan chain design perspective, three approaches exist for 3D ICs: (1) independent design per layer with separate chains; (2) mapping the 3D problem to 2D for simplified solution; and (3) true 3D optimization considering differences between horizontal and vertical interconnects based on 3D Manhattan distance. The first approach requires no modification to existing 2D scan design algorithms but may result in excessive TSV counts by ignoring vertical connections. The second approach similarly allows direct use of 2D algorithms but also neglects TSV costs. The third approach represents a genuine 3D scan design methodology but requires modifying 2D algorithms and incurs higher computational overhead. The underlying algorithms can be formulated as linear programming problems [**?**].

Beyond scan design, test access mechanisms and test scheduling must also consider co-optimization. Die-level testing requires determining test pin allocation for each core, while post-integration testing needs a different allocation scheme. To minimize individual test costs, these allocation methods may differ. Implementing two separate test access mechanisms would incur unacceptable area overhead, necessitating a unified test access mechanism and scheduling algorithm that minimizes total test cost across both pre- and post-bond phases.

A major challenge in 3D IC design is thermal management. Since multiple dies are directly stacked, heat dissipation becomes difficult, particularly at the center where temperatures can become very high. Test scheduling must incorporate thermal constraints to guide core testing schedules. While this issue is primarily significant during post-bond testing, it is less critical during pre-bond testing.

5 Conclusion

This paper has discussed the primary testing challenges facing 3D integrated circuits and potential solutions. We emphasize the critical importance of 3D IC testing, which stems not only from the technology' s broad adoption prospects but also from the fundamental challenges it poses that may necessitate disruptive changes to traditional testing methodologies. This field is likely to become a major research focus in the testing community over the next decade. We hope this analysis will attract more researchers to this area and accelerate progress in 3D IC testing research.

6 Acknowledgments

As a survey paper, this work inevitably references many viewpoints from the literature. We cite third-party work upon first reference but do not repeat citations for subsequent mentions of the same work. We also thank Chen Yuanqing from our research group for valuable feedback on this manuscript.

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