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Postprint: Delay Testability Design Techniques for Integrated Circuits

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Abstract

As the feature size of integrated circuit manufacturing processes continues to shrink, the timing constraints of high-performance integrated circuit products are becoming increasingly stringent. The impact of various manufacturing defects, such as resistive opens, resistive shorts, void formation in vias, and gate oxide failures, is also becoming increasingly significant under current advanced integrated circuit manufacturing processes. To ensure the outgoing quality of chips, effective delay testing is typically required. Design for delay testability of integrated circuits can not only effectively detect delay defects in chips, but also facilitate effective debugging before mass production. In this paper, we first introduce the impact of delay defects in integrated circuits on chip performance and reliability, and then respectively present several methods that employ delay testability design techniques to improve fault coverage of chip delay testing, reduce the scale of delay test vector sets, detect small delay defects in chips, and perform online detection of delay faults in chips.

Full Text

Preamble

Design-for-Delay-Testability Techniques in Integrated Circuits
Songwei Pei, Huawei Li

Abstract

As feature sizes of integrated circuit manufacturing processes continue to shrink, timing constraints for high-performance IC products become increasingly stringent. The impact of various manufacturing defects—including resistive opens, resistive shorts, void formation in vias, and gate oxide failures—has become more significant under advanced IC manufacturing processes. To ensure chip

quality, effective delay testing is essential. Design-for-delay-testability in integrated circuits not only efficiently detects delay defects but also facilitates effective debugging before mass production. This paper first introduces the impact of delay defects on chip performance and reliability, then presents several delay testability design techniques for improving delay test fault coverage, reducing delay test pattern size, detecting small delay defects, and enabling online detection of delay faults.

Keywords: delay testing, design for testability, small delay defect, fault coverage, delay measurement

1. Introduction

As integrated circuit manufacturing feature sizes continue to shrink, chip performance and complexity continue to increase [1]. In deep submicron regimes, phenomena such as resistive opens, resistive shorts, void formation in vias, and gate oxide failures have become increasingly common and significant, posing serious challenges to chip performance and reliability [2]. Moreover, process parameters like channel length, oxide thickness, and metal line width cannot be precisely controlled to their target values but instead vary within a range. Consequently, electrical parameters such as saturation current, threshold voltage, and resistance/capacitance exhibit large variations, ultimately causing significant delay variations in logic gates and signal propagation paths [3]. Therefore, as chip timing constraints become increasingly strict, testing whether chips function correctly at rated operating frequencies has become an indispensable step for ensuring quality [4,5], creating a demand for delay testability design.

First, using functional patterns for delay testing requires expensive external testers to apply these patterns at-speed and incurs high costs to develop functional pattern sets that achieve satisfactory delay fault coverage [6].

Furthermore, small delay defects (manufacturing defects causing minor additional delays) have become increasingly prevalent in deep submicron processes, yet traditional delay testing methods often struggle to detect them. Undetected small delay defects during chip testing may cause timing failures during normal functional operation if they affect signal propagation delays along very long functional paths. Even if small delay defects do not affect normal functionality, they pose serious reliability challenges during chip operation [2]. For example, a small void formed in a via during manufacturing may cause a minor delay that does not immediately affect functional paths but could eventually lead to an open circuit through electromigration failure, causing functional failure [7,8]. To detect small delay defects, many ATPG-based methods attempt to generate delay test patterns that sensitize long paths with small slack values (where slack is the difference between test clock period and path delay). However, this approach' s effectiveness depends on the distribution of path delays within the chip. On one hand, some nodes exist where even the longest paths through them have large slack values. On the other hand, the exponential growth of

paths with circuit size, delay variations, complex designs, and low path testability due to test constraints [5,9] make it difficult to select sufficient testable long paths. At-speed testing provides a more effective means for detecting small delay defects, but implementing at-speed delay testing through high-speed external testers is extremely expensive. Moreover, test clock frequency is easily limited by stray parameters such as parasitic resistance, capacitance, and transmission line impedance [10,11,12].

Additionally, chips may experience transient delay faults during normal operation due to soft errors, crosstalk, and power supply noise. As chip integration increases, the probability of soft errors during normal operation continues to rise; growing coupling capacitance between interconnects leads to more severe crosstalk effects; and circuit delays become increasingly sensitive to voltage fluctuations. Therefore, for reliability-critical applications, online detection of functional failures is typically required [13,14], and designing on-chip delay violation detection circuits provides an important means for online functional failure detection.

In summary, relying solely on external testers for delay testing has become limited in effectiveness. Consequently, many researchers have investigated on-chip delay testability design techniques to effectively improve delay fault coverage, reduce test pattern size, detect small delay defects, and enable online delay fault detection. The following sections introduce several recent related delay testability design techniques.

2. Delay Testing Technology Based on Hybrid Scan

Scan-based delay testing methods are generally very effective for chip delay testing. To test whether a node has a transition fault, a test pattern pair <V1,V2> is applied to the circuit-under-test. The first pattern (initialization vector V1) initializes the internal logic to a known state; the second pattern (launch vector V2) creates transitions at circuit inputs to excite and propagate the target fault effect, detecting delay faults by capturing the circuit response after the rated clock period. V1 is typically shifted in using a slow scan test clock. Based on how V2 is obtained, common delay testing methods are classified as Launch-on-Capture (LOC), Launch-on-Shift (LOS), and Enhanced Scan [5].

In LOC, V2 is obtained by capturing the circuit response to V1 during the capture clock cycle. This approach has minimal implementation cost but suffers from structural constraints when obtaining V2, making many transition faults undetectable because no circuit state can excite and propagate their effects to observable outputs. Consequently, LOC delay testing has relatively low fault coverage.

In LOS, V2 is obtained by shifting V1, but this requires an at-speed scan enable signal, making hardware implementation difficult and thus rarely adopted in most scan-based designs. Additionally, the shift dependency between V2 and V1 limits transition delay fault coverage.

Enhanced scan delay testing can simultaneously store two bits in scan flip-flops, allowing V1 and V2 to have no structural constraints, achieving very satisfactory transition delay fault coverage. However, this requires significant hardware overhead to store two test bits without affecting the circuit state during shifting. Some researchers have combined this with LOC, using partial enhanced scan—replacing a very small percentage of general scan flip-flops with enhanced scan cells—to achieve satisfactory transition delay fault coverage with acceptable hardware overhead or to obtain very compact delay test patterns to reduce test cost.

[Figure 1: see original paper] shows one implementation of a scan chain structure with partial enhanced scan cells [15,16], containing both general and enhanced scan flip-flops. [Figure 2: see original paper] shows a common multiplexer-based general scan flip-flop [5]. Figure 3: see original paper and Figure 3: see original paper present two implementation schemes for enhanced scan flip-flops [15,16]. Enhanced scan cells have the same external pins as general scan flip-flops, facilitating integration into standard industrial design flows. Since enhanced scan cells can store two bits simultaneously, V2 does not depend on the circuit response to V1. The enhanced scan flip-flops in Figure 3: see original paper and Figure 3: see original paper have similar functionality. The operation of a scan chain with partial enhanced scan cells is analyzed by describing the functionality of the enhanced scan cell in Figure 3: see original paper.

[Figure 4: see original paper] shows the timing diagram for relevant signals of the enhanced scan cell from Figure 3: see original paper during operation [16]. Assuming all flip-flops are positive-edge triggered, when the circuit operates in normal functional mode, the scan enable signal remains low and, after clock initialization, the MUX Control signal also stays low. In this case, the enhanced scan cell functions equivalently to a general scan flip-flop, with combinational logic signals captured through the DI port. When scan enable is high, the scan chain enters shift mode, allowing state values to be shifted into both master and slave flip-flops of enhanced scan cells through the SI port. When obtaining V2 via LOC, general scan flip-flops in the chain capture their combinational logic responses, while enhanced scan cells (with internal MUX control remaining high) capture the corresponding V2 bits from their slave flip-flops in the master flip-flop, effectively improving transition delay fault coverage [16].

To keep area overhead acceptable, an effective optimization method must replace only critical general flip-flops with enhanced scan cells. Research in [17] proposed using partial enhanced scan to improve path delay fault coverage, starting from full enhanced scan and sequentially replacing enhanced scan cells with general ones without reducing path delay fault coverage. In [16], controllability analysis of each general flip-flop was performed by applying random vectors (with 0.5 probability for each value) to primary and pseudo-inputs (flip-flop outputs), using Monte Carlo simulation or controllability analysis to determine the probability of setting each flip-flop to 0 or 1. Flip-flops with large probability deviations from 0.5 were replaced with enhanced scan cells. However, probability

calculations have significant errors, and simple probability-based controllability analysis has weak correlation with transition delay fault coverage, requiring extensive adjustments to achieve high coverage.

In [18], a selection algorithm replaced general scan flip-flops with enhanced ones based on the set of transition delay faults undetectable by LOC but detectable by enhanced scan, aiming to improve fault coverage with small area overhead. However, this method did not consider sensitized propagation paths for transition delay faults. In [15], controllability and usefulness analysis of general scan flip-flops proposed a selection algorithm for replacing general flip-flops with enhanced ones to reduce delay test pattern size. Additionally, partial enhanced scan also improved transition delay fault coverage.

By studying the relationship between flip-flops and fault detection, we proposed two flip-flop selection methods for effectively improving transition fault coverage [19] and reducing test pattern size [20]. In [19], based on the set of LOC-undetectable but enhanced-scan-detectable transition delay faults, we calculated the correlation between undetectable faults and general scan flip-flops, replacing critical general flip-flops with enhanced ones to improve coverage. In [20], based on redundant fault analysis and transition fault compaction, we defined activation correlation and sensitization correlation concepts. Using calculations of activation correlation, sensitization correlation, and controllability of general scan flip-flops, we established a selection function to replace critical general flip-flops with enhanced ones, effectively reducing delay test pattern size.

3. On-Chip Delay Measurement Technology

Applying design-for-testability techniques for on-chip path delay measurement not only effectively detects delay defects but also facilitates pre-production debugging [21,22]. To measure a specific path' s delay on-chip, single-path-sensitizable delay test patterns are generated to introduce transition signals at the path' s start and end points into on-chip delay measurement units. [Figure 5: see original paper] shows a simple implementation of on-chip delay measurement technology [25], where BIDM (Built-In Delay Measurement) represents the on-chip delay measurement device. Transition signals at the path' s input and output ports are selected through multiplexers or encoders/decoders into the BIDM unit for path delay measurement. Results are obtained through the Delay Readout port in the BIDM circuit [21]. The measurement path' s inputs and outputs can be primary inputs, pseudo-inputs, primary outputs, and pseudo-outputs (flip-flop inputs). For easier testing and debugging, internal circuit nodes can also be selected as path inputs or outputs for on-chip BIDM measurement [21]. Several recent digital on-chip delay measurement circuits are described below [23].

3.1 Implementation Using Vernier Delay Line Principle

[Figure 6: see original paper] shows an on-chip delay measurement implementation based on the vernier delay line principle [24]. This method contains two balanced buffer chains. Assuming the upper chain (connected to port y) has buffer delay Dy and the lower chain (connected to port x) has smaller delay Dx, the path-under-test’ s start and end points connect to ports y and x respectively. If a rising transition is applied at the path input, after the path delay, the output produces a similar rising transition. When the delay difference between these two transitions is sufficiently large, the first flip-flop nearest to ports x and y will latch a logic high.

As the two transitions propagate along the buffer chains, their delay difference gradually decreases with each stage. If the measurement range is sufficiently large, some flip-flops will fail to meet setup time requirements and remain at the initialized logic low. The number of flip-flops latched high indicates the measured path delay. The measurement resolution TR of this vernier-based method is:

TR = Dy - Dx

Unlike single-buffer-chain methods, this approach avoids resolution degradation from buffer delays in specific processes. Theoretically, this method can measure paths with arbitrary delay magnitudes.

In [22], conventional scan flip-flops were enhanced with two multiplexers to create delay scan flip-flops, as shown in [Figure 7: see original paper]. When the delay_scan signal on the delay scan chain is high, transitions at ports y and x (connected to the path-under-test’ s input and output) are sent to the delay scan flip-flops to begin measurement. When delay_scan is low, these flip-flops function as conventional scan flip-flops. This structure still uses the vernier delay line principle for on-chip delay measurement.

In [21], an improved vernier method divides the measurement circuit into coarse-grain modules with large measurement range per stage and fine-grain modules with small range per stage, as shown in [Figure 8: see original paper]. Transitions at the path’ s start and end points enter through reference (Ref) and data (Data) ports into calibration circuits and glitch-reducing Schmitt trigger circuits, then through specially designed dynamic-logic gates (DG) that convert them to rising transitions for the coarse-grain differential delay line. Delays smaller than the coarse resolution are further measured by the fine-grain differential delay line.

To reduce area overhead, we proposed an on-chip path delay measurement circuit structure for delay fault detection and debugging [25], shown in [Figure 9: see original paper]. This circuit uses multi-stage delay measurement units with exponentially increasing resolution from the last stage to the first. The delay difference between two transitions is calculated from the binary number formed by flip-flop values in each stage. Compared to vernier delay line methods, this

approach measures larger delay ranges with fewer stages, significantly reducing measurement time and area overhead while improving resolution and accuracy.

3.2 Technology Based on Asymmetric Inverters

[Figure 10: see original paper] shows an on-chip delay measurement method using asymmetric inverter delay lines [26]. Figure 10: see original paper shows a pulse generator (essentially an XOR gate). Figure 10: see original paper shows two asymmetric inverter circuits. Assuming rising transitions at the path-under-test' s start and end points connect to signals x and y in Figure 10: see original paper, pulse shaping occurs as shown in Figure 10: see original paper. Figure 10: see original paper shows the delay measurement structure using asymmetric inverter delay lines. Each pulse shaping stage is shown in Figure 10: see original paper. The asymmetric inverter unit contains two asymmetric inverters: the first has a wide PMOS transistor (m times the NMOS width), and the second has a wide NMOS transistor (m times the PMOS width). When a falling transition enters the unit, the first inverter' s output rises quickly due to the large PMOS, and the second inverter' s output falls quickly due to the large NMOS. This progressively narrows the pulse width through each asymmetric inverter stage. When the pulse becomes sufficiently narrow, it cannot latch the desired logic value into flip-flops. The path delay is determined by the pulse width reduction per stage and the logic values latched in each flip-flop.

3.3 Implementation Using Ring Oscillator Principle

[Figure 11: see original paper] shows an on-chip path delay measurement method using ring oscillator principles [27]. The measurement and calibration unit (MC) in Figure 11: see original paper can adjust delay values. The calibration launch flip-flop (CLFF) and calibration capture flip-flop (CCFF) in Figure 11: see original paper and Figure 11: see original paper are modified from conventional flip-flops to enable ring oscillation between the path-under-test and the CLFF-to-CCFF path. The operation principle is: first generate a delay test pattern for the path from CLFF through MC to CCFF, then use MC' s control scan chain to adjust its delay. By determining pattern pass/fail, set the CLFF-to-CCFF path delay to exactly one clock period, denoted as T_cmc. As shown in Figure 11: see original paper, (b), and (c), when the oscillation enable signal OE is active, transitions can resonate in a loop between the path-under-test and the CLFF-to-CCFF path. If a transition traverses this loop 2N times in time T, the path delay T_path is:

$$T_{path} = (T / (2N)) - T_{cmc}$$

4. On-Chip At-Speed Delay Test Technology

On-chip at-speed testing generates adjustable-frequency test clocks internally to test chips at higher frequencies than functional clocks, reducing path slack values to effectively detect small delay defects.

T. McLaurin and F. Fredrick [28] proposed a method using on-chip PLL-based clock control circuits for at-speed testing, but this requires PLL reset before each test pattern, making it impractical.

R. Tayade and J. A. Abraham [12] proposed an on-chip programmable capture signal (CAPTURE) generator, shown in [Figure 12: see original paper], enabling path delay measurement by adjusting test clock periods. Figure 12: see original paper shows the programmable capture signal generator. By adjusting scan flip-flop clock selector values, the transition at test trigger (TT) can control the delay between CAPTURE and TT signals through coarse-grain and fine-grain delay units, thereby adjusting the test clock frequency by changing the delay between launch and capture clocks. Based on this generator, hardware structures for LOC, LOS, and enhanced scan delay testing were implemented. Figure 12: see original paper shows the enhanced scan implementation, easily adaptable to LOC and LOS. Figure 12: see original paper shows the clock signal selector. The scan chain includes an enhanced scan cell that, when a test pattern is applied, generates a rising transition at TT during the launch event. This transition adjusts the test clock period through the programmable capture generator. When FCLK_STOP is high and SE is low, CAPTURE is sent to CLK. Thus, adjusting the delay between CAPTURE and TT changes the test clock period, enabling on-chip at-speed delay testing.

5. Online Delay Fault Detection Technology

Chips require effective testing before shipment to ensure correct operation at rated frequencies. However, during operation, chips may experience transient delay faults from soft errors, crosstalk, and power supply noise, and aging effects can increase delays, eventually causing functional failure. For critical applications, online functional failure detection during normal operation is required.

K. Raahemifar and M. Ahmadi [29] proposed a circuit structure for online delay fault detection in functional mode, shown in Figure 13: see original paper. Assuming Φ1 is the clock signal and S is combinational logic output, the detection principle monitors combinational logic output stability—checking whether outputs have stabilized before the clock edge arrives. For negative-edge-triggered flip-flops, the stability detection circuit in Figure 13: see original paper is inserted at combinational logic outputs. When the clock is high, transistor N2 conducts, making Out and Od maintain identical logic values regardless of the combinational output. After the falling clock edge, defect-free chips should have stable combinational outputs. When the clock is low, N2 turns off, and Out and Od retain their previous logic states. If combinational outputs transition while the clock is low, Out or Od changes, and XORing them detects delay faults online. Figure 13: see original paper operates similarly.

Based on the stability detection principle in Figure 13: see original paper, references [13,14] proposed methods for predicting and detecting chip failures. Assuming positive-edge-triggered flip-flops, CLK is the clock signal, and CO and

COV are combinational logic output and its complement. When CLK is low, transistors M1 and M2 conduct while M5 is off, making S1 and S2 logic high regardless of CO and COV. These feed a NOR gate producing low OUT. This precharge phase occurs before the rising clock edge. If the chip has no delay faults, combinational outputs stabilize to final values before the edge, keeping OUT low. If combinational outputs transition when CLK is high, both S1 and S2 become low, making OUT high. Thus, analyzing OUT enables online delay fault detection.

6. Conclusion

This paper introduced several delay testability design techniques for integrated circuits. These techniques effectively improve transition delay fault coverage, reduce test pattern size, detect small delay defects, and enable online delay fault detection. Overall, research focuses on achieving satisfactory fault coverage and ideal test pattern size with smaller area overhead to improve test quality and reduce test time. Another focus is designing high-precision on-chip delay measurement circuits or high-speed test signals with reasonable area overhead to effectively detect small delay defects, avoiding expensive external high-performance testers. Effective delay testing has long been an industry challenge, and design-for-delay-testability techniques will continue receiving attention as an important solution approach.

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