Large-Scale Photonic Integrated Chip Postprint

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Abstract

Computers represent a crucial milestone in humanity' s transition to the information age and serve as a fundamental pillar supporting information technology. Since the 1960s, unprecedented achievements have been accomplished in the field of electronic computing. However, current computer development confronts two critical bottlenecks—speed and power consumption—which have engendered three technical barriers impeding performance advancement: the power wall, memory wall, and I/O wall. Energy consumption constitutes the foremost technical obstacle constraining high-performance computing development. Based on existing technological trajectories, exascale systems will exhibit power consumption of 466.7 MW and annual electricity usage of 4.088 billion kWh, equivalent to one-twentieth of the Three Gorges Dam' s total generation in 2014. Furthermore, information exchange speeds between processors and memory (memory access) and among processors (I/O) substantially lag behind computational speeds, with memory access and I/O bottlenecks limiting processor performance to merely 10% of its potential, thereby imposing severe constraints on computing advancement. Conventional chip feature size reduction, constrained by fundamental physical limits of electrons, cannot resolve these issues and may indeed aggravate them.

Full Text

Preamble

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Large-Scale Photonic Integrated Chips

1. Project Background

Computers represent a hallmark of humanity' s entry into the information age and serve as a critical pillar supporting information technology. Since the 1960s, unprecedented achievements have been made in electronic computing; however, current computer development now faces two fundamental bottlenecks: speed and power consumption. These have given rise to three technical barriers impeding performance improvements—the power wall, memory wall, and I/O wall. Energy consumption represents the greatest technical obstacle to high-performance computing development. Based on existing technologies, an exascale system' s power consumption would reach 466.7 MW, with annual electricity usage of 4.088 billion kWh, equivalent to one-twentieth of the Three Gorges Dam' s total 2014 power generation. Furthermore, the speed of information exchange between processors and memory (memory access), as well as between processors themselves (I/O), severely lags behind processor computing speeds. These memory and I/O bottlenecks limit processor performance to merely 10% of its potential, imposing severe constraints on computing development. Traditional chip feature size reduction, constrained by the physical limits of electrons themselves, cannot resolve these issues and may even exacerbate them.

Compared to electrons, photons offer ultra-high transmission speeds, ultra-high parallelism, ultra-high bandwidth, and ultra-low transmission and interaction power consumption. Therefore, utilizing photonic chips for information exchange and computation represents a key strategy for overcoming electronic computer development bottlenecks. Moreover, photonic chips constitute a pivotal enabling technology for the entire future information domain, with profound market and strategic significance in information technology, national defense, energy, and healthcare sectors [Figure 1: see original paper].

Photonic integrated chips have achieved rapid development since 2000, transitioning from discrete devices to large-scale integration. Currently, large-scale photonic integrated chips have become one of the most competitive international research arenas, with the United States, European Union, and other developed nations incorporating photonic integration industries into their national strategic plans. For instance, in October 2014, President Obama announced the establishment of the "National Integrated Photonics Manufacturing Innovation Institute" dedicated to transforming end-to-end photonics ecosystems. In July 2015, a presidential executive order promoted research, development, and deployment of national strategic computing (high-performance computing). Industrial giants led by IBM and Intel, as well as academic leaders including MIT and UCSB, are vigorously developing large-scale photonic integrated chips. In 2015, MIT and multiple universities published a paper in *Nature* on large-scale photonic integrated chips integrating 850 devices.

Against this international backdrop of rapid large-scale photonic integrated chip development, China faces enormous challenges alongside significant opportunities. According to customs statistics, in 2013 China' s integrated circuit chip

imports reached $231.34 billion, surpassing crude oil to become the nation' s largest import commodity. Following the Snowden revelations, China has more fully recognized that massive core chip imports pose a tremendous hidden threat to national security. Currently, the commercial photonic integrated chip industry is still in its infancy internationally. As a new integration technology independent of electronic integration, technical barriers have not yet been fully established, providing China with sufficient market space and R&D time for large-scale photonic integrated chips, as well as tremendous opportunities for China' s information industry. In summary, large-scale photonic integrated chips represent a critical technology for resolving computer development bottlenecks, currently constitute the most competitive international research field, and possess strong forward-looking significance, radiating effects, and driving force.

China has accumulated rich experience and technology in basic discrete devices, and the timing is ripe for launching large-scale integration technology research. There is an urgent need to initiate research on large-scale photonic integrated chips to provide technical reserves for China to seize the international high ground in information technology in the future.

2. Scientific Issues and Objective Planning

Utilizing photons to break through technical barriers in computer development still faces a series of challenges, arising not only from computer architecture limitations but more importantly from constraints in material and device functionality, integration, miniaturization processes, and large-scale integration technologies. Therefore, we must start from fundamental photonic integration theory, continuously explore and investigate the physical 内涵 of new phenomena and laws, and breakthrough materials, devices, and chip integration processes and technologies to drive the transition from electronic computing to optoelectronic hybrid computing and even quantum computing.

The "Large-Scale Photonic Integrated Chips" Strategic Priority Program targets the international frontier of large-scale photonic integrated chips, focuses on major demands in high-performance computing, aligns with national information technology development strategies, and leverages the Chinese Academy of Sciences' strengths in photonics, integrated optics, and high-performance computing. Through fundamental theoretical research in photonic integration, the scientific objective is to establish a theoretical framework for describing and manipulating photon behavior at high density and small scales. The core technical objective is to breakthrough large-scale integration processes and technologies, and construct a process platform for large-scale photonic integration materials, devices, integration, and packaging [FIGURE:2, FIGURE:3].

Adhering to the principle of focused objectives and key breakthroughs, this program, based on foundational science and technology breakthroughs, will focus on developing the world' s first large-scale photonic integrated processing proto-

type chip with 1.6 Tbps real-time parallel memory access capability, 3.2 Tbps interconnect and switching capacity, and 5 trillion matrix multiply-accumulate co-processing operations per second. The prototype will undergo functional verification using massively parallel processing (MPP) architectures in high-performance computing to promote sustainable high-performance computing development. Simultaneously, the program will conduct fundamental research on quantum optical chip integration to provide hardware support for future quantum computer research.

This program is led by the Xi' an Institute of Optics and Precision Mechanics, Chinese Academy of Sciences, in collaboration with the Institute of Semiconductors, Shanghai Institute of Microsystem and Information Technology, and Institute of Computing Technology of the Chinese Academy of Sciences. Based on the overall chip objectives [Figure 4: see original paper] and leveraging each unit' s advantages in photonic technology, III-V semiconductor technology, IV semiconductor technology, and computational science, the program has deployed five projects with task divisions shown in [Figure 5: see original paper].

The five projects are coordinated and rationally distributed by the partner units according to their respective strengths, completed through close collaboration. Relevant research topics are established within each of the five projects to conduct targeted research, with each topic undertaken by an independent unit. The core personnel undertaking the program consist of mid-career and young researchers from both domestic and international backgrounds, with 骨干 members selected from talent programs including the "Thousand Talents Plan," "Foreign Expert Thousand Talents Plan," "Outstanding Youth Fund," "Hundred Talents Program," "Young Thousand Talents Plan," and "New Century Talents Project." The research team possesses solid theoretical foundations and strong technical accumulation in photonic integration and device R&D.

Project 1: Silicon-based hybrid high-speed optical memory access core unit, undertaken by the Institute of Semiconductors, to achieve 1.6 Tbps high-speed processor-memory access functionality and break through the memory wall constraint.

Project 2: High-bandwidth on-chip optical interaction unit, undertaken by the Shanghai Institute of Microsystem and Information Technology, to achieve 3.2 Tbps multi-processor information exchange functionality and break through the I/O wall constraint.

Project 3: Optical computing and optical quantum chip fundamentals and technology research, undertaken by the Xi' an Institute of Optics and Precision Mechanics, to achieve 5 trillion optical matrix operation core functionality while exploring large-scale integrated devices and processes for optical quantum chips.

Project 4: Large-scale photonic integrated chip integration technology research, undertaken by the Xi' an Institute of Optics and Precision Mechanics, serving as the overall chip system integration to achieve multi-device, multi-material, and multi-functional unit chip-level integration.

Project 5: Large-scale photonic integrated chip prototype verification system, undertaken by the Institute of Computing Technology, responsible for exploring optoelectronic hybrid computing models and prototype chip computing system verification.

3. Expected Outcomes

Building a large-scale photonic integrated science and technology system is a complex systematic engineering effort requiring strategic planning and long-term investment. Partner units in the "Large-Scale Photonic Integrated Chips" Strategic Priority Program will progressively breakthrough core chip-level device technologies including multi-material fusion, high-performance on-chip light emission and detection, on-chip high-order modulation, and low-loss passive circuits, while accumulating and mastering key processes for large-scale device fabrication, integration, and packaging. The program will focus on breakthroughs in super-node chips for large-scale parallel computing systems oriented toward high-performance computing, while radiating comprehensively into information fields including communications and sensing. Over the next 10-15 years, through strengthened collaboration with renowned domestic and international enterprises, the program will successively launch series of photonic integrated chips for high-speed optical access, large-capacity optical transmission in data centers, massive coherent optical communications in backbone networks, and high-speed on-chip optical interconnect/optical switching, breaking the current situation where China' s high-end processing chips in the information field are almost entirely import-dependent and positioning China as a strong competitor in the future international optical information market. Through this program' s implementation, the following research outcomes are expected:

(1) **Theoretical Innovation:** Propose and refine the theoretical system for optoelectronic hybrid computing and construct hybrid computing architectures.

(2) **Performance Optimization:** Use optical computing, optical transmission, and optical interconnects to break through development bottlenecks in electronically-dominated high-performance computers, explore optimal boundaries between optical and electrical domains (including computing and interconnect), and achieve optimal system energy efficiency.

(3) **Application Enhancement:** Perfect large-scale photonic integration theory, breakthrough core technologies in materials, devices, and large-scale integration, realize optoelectronic hybrid large-scale parallel computing system node chips, and substantially increase information interaction bandwidth density for short-distance transmission.

(4) **Scale Production:** Achieve large-scale integration processes and methods for multiple photonic devices on quantum chips.

(5) **Research Cluster Construction:** Establish an internationally first-

class large-scale photonic integrated chip R&D platform, unite CAS and domestic institutions' research strengths in photonic integration, and strive to build an internationally influential photonic integrated chip research community.

(6) **Cultivate Core Leading Talent:** Cultivate a group of internationally influential leading talents in both academic and industrial aspects, achieve cluster effects in the photonic integration field, and enable China to possess direct international competitiveness in the photonic chip domain.

Note: Figure translations are in progress. See original paper for figures.