Physical Layer Design for the RF Channel of the Quantum Science Experiment Satellite (Post-print)

Authors: Wang Zhugang, Xiong Weiming, Qu Chenyang, Chen Qiaoyan

Date: 2017-01-22T00:00:00+00:00

Abstract

The payload laser link of the quantum science satellite requires a classical high-speed uplink/downlink RF communication link for verification and comparison with the laser link. This paper presents the physical layer hardware design and algorithm design of the uplink/downlink RF link for the quantum science satellite. The link employs SRRC-OQPSK compliant with CCSDS spectral specifications as the uplink modulation type, with an uplink data rate of 1.024 Mbps; the downlink utilizes SRRC-OQPSK and GMSK modulation, achieving a data rate of 4 Mbps. Interfacing test results with multiple ground stations demonstrate that the data transmission transceiver achieves a carrier acquisition sensitivity better than -100 dBm, a data demodulation sensitivity better than -98 dBm, an AGC capability greater than 43 dB, and an actual transmission bit error rate better than 1×10 under a received signal level condition of -96 dBm. Experimental results demonstrate that the RF channel physical layer design scheme satisfies the requirements of the quantum science experimental mission.

Full Text

Physical Layer Design of Microwave Communication Link for Quantum Science Experiment Satellite

Zhugang Wang[1],[2],[3], Weiming Xiong[1],[3], Chenyang Qu[1], Qiaoyan Chen[1]

[1]National Space Science Center, Chinese Academy of Sciences, Beijing 100190, China
[2]University of Chinese Academy of Sciences, Beijing 100049, China
[3]Key Laboratory of Electronics and Information Technology for Space Systems, Chinese Academy of Sciences, Beijing 100190, China

Abstract

The laser link payload of the quantum science satellite requires a classical high-speed RF communication link for verification and comparison. This paper presents the physical layer hardware design and algorithm design of the uplink and downlink RF channels for the quantum science satellite. The uplink employs SRRC-OQPSK modulation compliant with CCSDS spectrum specifications at a data rate of 1.024 Mbps, while the downlink utilizes both SRRC-OQPSK and GMSK modulation at 4 Mbps. Joint testing with multiple ground stations demonstrates that the data transmission communication device achieves a carrier acquisition sensitivity better than -100 dBm, a data demodulation sensitivity better than -98 dBm, and an AGC capability exceeding 43 dB. Under a received signal level of -96 dBm, the actual transmission bit error rate is better than 1×10 . The measured results confirm that the RF channel physical layer design meets the requirements of the quantum science experiment mission.

Keywords: satellite communication, high-speed uplink, square root raised cosine-offset quadrature phase shift keying (SRRC-OQPSK), Gaussian minimum shift keying (GMSK)

0. Introduction

The data transmission communication device of the quantum science experiment satellite serves as supporting equipment for its payload, establishing a classical RF communication link between space and ground to verify the correctness and validity of quantum communication experimental data [1]. In conventional satellite uplink and downlink designs, the satellite platform transponder can transmit uplink telecommand and downlink telemetry data, but only at kbps-level rates. Typical detection and Earth observation payloads only require high-speed downlink data transmission, so conventional payload data transmission equipment merely performs downlink data modulation and amplification without the capability to receive high-speed uplink data.

The data transmission communication device for the quantum science experiment satellite not only accomplishes the high-speed downlink data transmission functions of conventional equipment but also provides high-speed uplink data reception and demodulation, as well as uplink and downlink data link layer encoding/decoding and large-capacity storage of downlink data.

The physical layer and data link layer specifications of the communication device comply with CCSDS standards [2]: S-band for both uplink and downlink; uplink channel data rate of 1.024 Mbps with SRRC-OQPSK modulation (roll-off factor = 0.5), bit error rate better than 1×10 , and RS(255,223) channel coding without interleaving. Downlink channel rate of 4 Mbps with SRRC-OQPSK modulation (roll-off factor = 0.5) and GMSK modulation (BTb = 0.5), RS(255,223) channel coding with two-level interleaving, output average power greater than 36 dBm (4 W), and EVM better than 10%.

This paper focuses on the physical layer design of the quantum science experiment satellite data transmission communication device, excluding the power amplifier, covering the RF transceiver module architecture, modulation and demodulation algorithms, and hardware implementation platform.

1.1 RF Module Overall Architecture

Various architectures are available for downconverting S-band RF signals to frequencies acceptable by the baseband processing unit (primarily comprising ADC and FPGA) and upconverting baseband signals to S-band. These include superheterodyne structures, zero-IF and low-IF structures with quadrature frequency conversion, as well as Hartley and Weaver structures that can suppress image frequencies without RF filters [3].

Except for the superheterodyne architecture, all other RF architectures require quadrature local oscillators. However, phase and amplitude imbalances in quadrature LOs, along with gain mismatches between in-phase and quadrature branch amplifiers, adversely affect modulation and demodulation performance. Consequently, the quantum communication equipment adopts a superheterodyne structure.

The data transmission communication device for the quantum science experiment satellite employs an optimized integrated transmit-receive design that shares a common local oscillator. The two outputs of the LO are simultaneously fed to the receive downconverter and transmit upconverter. The overall RF module architecture is illustrated in Figure 1 [Figure 1: see original paper].

In Figure 1, LNA denotes low-noise amplifier, BPF1 is the receive bandpass filter, BPF2 is the intermediate frequency filter, AGC is the automatic gain control amplifier, LO is the local oscillator, LPF is the image-rejection low-pass filter at the DAC output, AMP is the transmit IF amplifier, BPF3 is the transmit frequency bandpass filter, and PA is the power amplifier. Modules with arrows in between represent isolators. The primary chip in the baseband processing unit is an FPGA (Field-Programmable Gate Array). TCXO stands for temperature-compensated crystal oscillator; while Figure 1 shows its output connected directly to the DAC, in the actual circuit it is multiplied within the FPGA before being output to the FPGA.

In the diagram, an isolator is placed between the LO output and the transmit mixer to prevent interference from transmit signals to receive signals.

1.2 Component Parameter Selection and Design

Based on the design requirement of a shared LO for transmit and receive, the selection of LO frequency and transmit/receive IF must consider the following factors: a) The transmit filter for image rejection must achieve -40 dBc suppression with stopband distance from center frequency 40 MHz; b) DAC device refresh rate 400 MHz; c) Processable output rate of baseband processing unit

(FPGA) 150 MHz; d) Analog bandwidth of receive-end ADC 475 MHz; e) Sampling rate of receive-end ADC 100 Msps.

According to these design requirements, the reference source frequency and transmit/receive IF parameters are selected as follows: - LO frequency: 22xx MHz - Receive IF frequency: 134 MHz - IF filter 3 dB bandwidth: 7 MHz - Crystal reference source frequency: 64 MHz - ADC sampling frequency: 64 MHz - Transmit IF refresh rate: 144 MHz - Center frequency: 47 MHz

The 3 dB bandwidth of the receive IF filter is 7 MHz, significantly wider than the signal bandwidth (uplink signal baseband rate of 1.024 Mbps with -30 dBc signal bandwidth of 768 kHz). Consequently, the uplink signal and substantial out-of-band noise enter the ADC simultaneously, with subsequent digital signal processing performing out-of-band noise filtering.

After allocating gain parameters to each component and inputting them into system design software, the calculated overall noise figure and third-order intermodulation of the RF module are shown in Figure 2 [Figure 2: see original paper].

The simulated system performance yields: system noise figure 2 dB, SNR 7.5 dB, third-order intermodulation product at -38 dBm, and SFDR of 17.8 dB.

When a single-carrier test signal passes through the filter and AGC, the spectrum of the IF signal output to the IF processing board is shown in Figure 3 [Figure 3: see original paper]. C/N measurements of the IF signal verify the microwave simulation software calculations.

2. Modulation Algorithm

The modulation principle of OQPSK signals is essentially identical to that of QPSK signals, with the sole distinction being the addition of a half-chip-period delay circuit in the Q branch. The implementation principle is illustrated in Figure 4 [Figure 4: see original paper]. If conventional FIR filter implementation is adopted for the shaping filter, an upsampling structure is required, consuming substantial FPGA resources such as multipliers. For direct-form FIR filters, the multiplier consumption in any branch equals the order of that branch's FIR filter. In this data transmission communication device design, multiple symbols from the I/Q branches are buffered and stored, then combined with the upsampling clock as lookup table indices to retrieve pre-stored multi-symbol waveform data. The final modulation algorithm implementation is shown in Figure 5 [Figure 5: see original paper].

The quantum science satellite is the first domestic satellite to adopt GMSK for downlink data transmission modulation. GMSK is one of the CCSDS-recommended downlink modulation schemes, featuring constant envelope characteristics suitable for saturated power amplifiers and rapid spectral roll-off. The GMSK principle involves filtering the rectangular frequency pulses of MSK

with a Gaussian impulse response filter having a modulation index of 0.5 before carrier modulation. Its implementation structure employs a multi-symbol lookup table architecture similar to that of SRRC-OQPSK signals. The final constellation diagrams of the downlink modulated signals are shown in Figures 6 [Figure 6: see original paper] and 7 [Figure 7: see original paper]. As evident from Figures 6 and 7, both signals exhibit monotonically decreasing spectral sidebands, providing faster roll-off rates compared to unshaped QPSK signals.

3.1 Demodulation Algorithm Design Tools and Flow

The demodulation algorithm design utilizes Matlab' s Simulink tool to simulate the performance of algorithm modules with different structures and parameters. The specific workflow involves: first verifying floating-point algorithm performance, then completing manual fixed-point design following empirical procedures, and finally validating fixed-point algorithm performance. Each module of the verified fixed-point algorithm has a corresponding FPGA module or IP core. After manual translation and mapping to VHDL code, the algorithm' s performance remains identical to the simulation results.

3.2 Digital Spectrum of Analog Intermediate Frequency

The center frequency of the signal output from the RF module to the IF processing unit is 134 MHz, while the ADC sampling frequency is 64 MHz. According to bandpass sampling principles, the resulting digital IF center frequency after ADC sampling is 6 MHz (134 - 64×2 = 6 MHz). The simulated digital IF signal spectrum is shown in Figure 8 [Figure 8: see original paper]. As seen in Figure 8, bandpass sampling causes noise folding at zero frequency. The amplitude of signal plus noise may occasionally exceed the ADC full scale, resulting in elevated noise sidebands in the digital IF.

3.3 Algorithm Framework Structure

The IF signal processing algorithm architecture is shown in Figure 9 [Figure 9: see original paper]. The top row represents the receive-side algorithms executed sequentially from left to right, while the bottom section shows the modulation algorithms. Both receive and transmit algorithms are monitored by several status parameters and intermediate state monitoring modules.

On the receive side, frequency offset detection and tracking modules are eliminated to accommodate the uplink signal acquisition mode and reduce resource consumption. Consequently, bit synchronization cannot operate under large frequency offsets and must be placed after carrier synchronization. Although joint carrier tracking and bit synchronization could yield better bit error rate performance, it might substantially increase loop lock-in time under extreme conditions. Therefore, the quantum satellite communication device' s uplink reception adopts a sequential architecture of carrier synchronization followed by independent bit synchronization.

Based on RF module design and calculations, the SNR after the IF filter is 7.5 dB under minimum input level conditions, and the analog AGC can effectively control input signal power. Test results show that across a 40 dB dynamic range of input RF signals and full temperature range, the IF signal dynamic range is only 2 dB. This control makes the IF signal dynamic range have minimal impact on acquisition and tracking performance. Therefore, omitting digital AGC in IF signal processing is satisfactory.

3.4 Uplink Signal Acquisition

The quantum science satellite operates in a low Earth circular orbit, generating approximately ±50 kHz Doppler frequency shift during entry and exit. To simplify the design for acquiring uplink signals with Doppler shift, a single-carrier sweep frequency and dual-acquisition mode similar to the satellite platform transponder is adopted between space and ground. The sweep signal characteristics are shown in Figure 10 [Figure 10: see original paper]. The frequency offset of the sweep signal provided by the ground station, when superimposed on the Doppler offset, produces a frequency deviation relative to the receiver center frequency ranging from -115 kHz to +115 kHz. When the ground station detects a valid "lock indicator" signal from the quantum satellite communication device via downlink telemetry or data transmission, it returns to the center frequency, leaving only the Doppler offset in the uplink signal.

The quantum satellite communication device employs a "waiting-for-rabbit" strategy to acquire sweep signals with Doppler shift. This strategy can be described as follows: when unlocked, the oscillation frequency of the limited carrier tracking PLL remains within ±6 kHz, a range that the uplink Doppler sweep signal covers during each sweep period. Once the quantum communication device locks onto the uplink, the limiting is removed. The corresponding PLL bandwidth must satisfy the requirement of capturing sweep signals at ±32 kHz/s while achieving a valid lock indication in much less than 0.3 seconds (12 kHz / (32 kHz/s) 0.3 s). This strategy prevents carrier tracking loop drift from expanding the sweep range and causing lock failure when no signal is present. Furthermore, implementing this strategy only requires adding a controllable limiter to the integral branch of the carrier tracking loop filter, resulting in minimal resource consumption.

3.5 Carrier Tracking

The carrier tracking loop employs a classic Costas loop structure, as shown in Figure 11 [Figure 11: see original paper]. Let the signal with phase offset be $s(t) = I(t)\cos(\omega_c t + \theta) + Q(t)\sin(\omega_c t + \theta)$, where I/Q are baseband symbols, θ is the phase offset, and $I, Q \approx \pm 1$.

The real expression of this complex signal is: $s(t) = \mathrm{Re}[(I(t) + jQ(t))e^{j(\omega_c t+\theta)}]$.

The signals on the two arms of the Costas loop are $I' = I\cos\theta - Q\sin\theta$ and

$Q' = I\sin\theta + Q\cos\theta$. The phase detector takes the form: $\theta_d = \text{sign}(I'Q' - Q'I')$.

From equation (2), the I/Q symbols disappear after the phase detector, yielding the phase error.

High-order matched filters consume substantial FPGA DSP and Slice resources. This design significantly reduces matched filter resource usage through two methods: first, downsampling the original 64 MHz rate to 4 MHz using a CIC filter; second, utilizing only a truncated portion (containing 99% of the total energy) of the SRRC matched filter length, reducing the SRRC filter order to 21. The SPAN=6 SRRC matched filter and the SPAN=2.8 truncation interval adopted in this design are shown in Figure 12 [Figure 12: see original paper].

The lock detector expression is [4]: $L = (I'^2 + Q'^2)^2 - 4I'^2Q'^2$.

The lock detector can also be expressed as the real part of the IF signal with phase offset raised to the fourth power. When the phase offset approaches zero (i.e., locked), the fourth power of any OQPSK constellation point lies on the real axis. The absolute value of this real component exceeds the lock threshold. Equation (3) shows that this detector works for both modulated signals and single-carrier signal lock detection. Since lock detection and phase detection occur before bit synchronization, numerous sampling points only approximate $I = Q \approx \pm 1$.

Both the lock detector and phase detector generate significant self-noise that must be filtered before use in phase locking and decision-making. The carrier tracking PLL loop bandwidth considers constraints such as sweep rate and loop stability, with the final design bandwidth set at 600 Hz.

3.6 Bit Synchronization

Bit synchronization, like carrier synchronization, employs a PLL-based feedback structure, as shown in Figure 13 [Figure 13: see original paper]. Its basic structure resembles the Gardner-type bit synchronization module with several adaptive modifications: First, since the sampling rate during bit synchronization is relatively high (approximately 7.8 samples/symbol), the interpolation filter is eliminated. Second, the timing error detector (TED) module adopts the ZE-TED form because carrier synchronization has already been achieved, eliminating the need for Gardner-TED' s rotation invariance. Additionally, the ZE-TED multiplier implementation requires no DSP units, reducing resource consumption. Finally, the TED module detects timing error from only one branch, with the timing output applied to both I and Q branches.

The performance characteristics of the communication device are summarized in Figure 14 [Figure 14: see original paper], showing both simulated and measured results. As seen in Figure 14, the simulated demodulation loss for the quantum satellite communication device is approximately 0.2–0.3 dB, while the measured demodulation loss is about 1.2–1.5 dB. The discrepancy between simulation and

measurement primarily arises because phase noise, sampling jitter, and third-order intermodulation caused by amplifier nonlinearity are not considered in the simulation.

3.7 Frame Synchronization and Descrambling

The uplink transmission frame of the quantum satellite communication device employs a 32-bit header compliant with CCSDS standards [5]. The frame synchronization design incorporates 1-bit header error tolerance, lock confirmation after 1 frame, and loss-of-lock confirmation after 0 frames.

The descrambling module uses the CCSDS-standard pseudo-random polynomial: $h(x) = x^8 + x^7 + x^5 + x^3 + 1$, which repeats every 255 bits.

4. IF Signal Processing Hardware

The IF signal processing hardware platform is a Xilinx FPGA, model XQR2V3000-4CG717V, with a main system clock of 64 MHz, core voltage of 1.5 V, and I/O voltage of 3.3 V. All its functions are depicted in Figure 9 [Figure 9: see original paper]. Mitigation measures for space radiation and single-event effects include triple modular redundancy (TMR) and pass reloading design. After partial TMR implementation, FPGA slice utilization reaches 87%, while other resource utilization remains below 80%. The system clock operates at 64 MHz, with a worst-case maximum clock frequency of 85.070 MHz, satisfying the 80% clock derating requirement.

5. Test Verification Results

Actual interface testing was conducted between a ground-based simulation transmitter and the developed engineering model of the spaceborne receiver. Receiver signal level measurements demonstrate a carrier acquisition sensitivity better than -100 dBm, a data demodulation sensitivity better than -98 dBm, and an AGC capability exceeding 43 dB. Link bit error testing reveals that under a received signal level of -96 dBm, continuous transmission of over 10^1 bits for 3.5 hours occurred without errors, indicating an actual transmission bit error rate better than 1×10 . The measured results confirm that the high-speed uplink design meets the requirements of the quantum science experiment mission.

Conclusion

This paper has presented the physical layer design of the quantum science experiment satellite data transmission communication device, excluding the power amplifier, covering the RF transceiver module architecture, modulation and demodulation algorithms, and hardware implementation platform. The RF module employs an optimized integrated transmit-receive design sharing a common local oscillator, whose two outputs are simultaneously fed to the receive downconverter and transmit upconverter.

The modulation algorithm adopts SRRC-OQPSK/GMSK efficient modulation techniques compliant with CCSDS specifications. The OQPSK modulation principle adds a half-chip-period delay circuit to the Q branch of QPSK modulation, with an implementation structure employing a multi-symbol lookup table architecture similar to SRRC-OQPSK signals, providing faster spectral roll-off compared to unshaped QPSK signals.

The IF signal processing hardware utilizes an FPGA, with triple modular redundancy and pass reloading design implemented to mitigate space radiation and single-event effects. After partial TMR, FPGA slice utilization is 87%, with other resource utilization below 80%.

In summary, this paper proposes a high-speed uplink solution with 1024 kbps transmission rate and channel bit error rate better than 1×10 , along with a 4 Mbps downlink, employing CCSDS-compliant SRRC-OQPSK/GMSK efficient modulation, RS(255,223) channel coding, and AOS bitstream service transmission protocol. This scheme satisfies the scientific experiment mission requirements of the quantum science satellite and provides valuable insights for engineering implementation of high-speed uplink data transmission systems in China.

References

[1] Weiming Xiong et al. Design of High-Speed Uplink for Scientific Experiment Satellites. Journal of Spacecraft TT&C Technology, 2013, 32(6): 518-523.

[2] CCSDS 401.0-B. Radio Frequency and Modulation Systems - Part 1: Earth Stations and Spacecraft, Blue Book [S]. Washington, D.C., CCSDS: 2011.

[3] Janine Sullivan Love. RF Front-End World Class Designs [M]. Netherlands, Elsevier: 2009.

[4] Peter W. Kinman, Jeff B. Bemer. Carrier Synchronization of Offset QPSK for Deep Space Telemetry [C]. IEEE Aerospace Conference, Big Sky, Montana, 9-16 Mar., 2002: 1327-1336.

[5] CCSDS 231.0-B-2. TC Synchronization and Channel Coding, Blue Book [M]. Washington, D.C., CCSDS.

Note: Figure translations are in progress. See original paper for figures.