ChinaRxiv 中X

AI translation · View original & related papers at
chinarxiv.org/items/chinaxiv-201612.00098

Analysis of Dynamic Resistance in the Drift Region of AlGaN/GaN HEMTs

Authors: Guohao Yu, Cai Yong, Wang Yue, Zhao Desheng, Zeng Chunhong, Hou Keyu, Dong Zhihua, Zhang Baoshun

Date: 2016-12-23T00:00:00+00:00

Abstract

AlGaN/GaN HEMTs are suitable for high-voltage high-power device applications; however, during high-voltage dynamic operation, there exists a phenomenon of increased on-resistance [1,2]. Currently, effective methods for reducing dynamic on-resistance include field-plate structures [3,4] and AlN dielectric layers [5], among others. This paper employs a stacked dual-gate structure AlGaN/GaN HEMT device, in which a top gate is newly added above the gate electrode, isolated from the gate electrode by a dielectric layer (Si3N4) and capable of independent signal control. During dynamic operation, the pulsed input signal of the top-gate electrode is synchronized with that of the gate electrode. In the device off-state, the top-gate electrode is biased at 0 V; in the device on-state, the top-gate electrode is biased at a positive voltage. The larger the positive voltage applied to the top gate in the device on-state, the smaller the dynamic on-resistance of the device.

Full Text

Preamble

AlGaN/GaN HEMT Drift Region Dynamic Resistance Analysis

Guohao Yu, Yong Cai, Yue Wang, Desheng Zhao, Chunhong Zeng, Keyu Hou, Zhihua Dong, Baoshun Zhang
Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, Jiangsu 215123, China
a) ghyu2009@sinano.ac.cn
b) ycai2008@sinano.ac.cn

AlGaN/GaN HEMTs are promising candidates for high-voltage, high-power applications, but suffer from increased on-resistance under dynamic high-voltage

operation [1,2]. Current effective methods for reducing dynamic on-resistance include field-plate structures [3,4] and AlN interfacial layers [5]. This work utilizes a stacked dual-gate AlGaN/GaN HEMT that incorporates an additional top gate above the main gate electrode, isolated by a Si N dielectric layer and capable of independent control. During dynamic operation, the pulsed signals applied to the top gate and main gate are synchronized. The top gate is biased at 0 V in the off-state and at a positive voltage in the on-state. Notably, the dynamic on-resistance decreases as the positive top-gate bias increases.

Device Structure

The device epitaxial structure consists of an AlGaN/GaN heterojunction grown by MOCVD on a 2-inch sapphire substrate, comprising a 2- m-thick GaN buffer layer, a 1-nm AlN interlayer, and a 30-nm Al . Ga . N barrier layer. Hall measurements reveal a 2DEG sheet density of 1.44×10^{13} cm ², electron mobility of 1080 $cm^2/V\cdot s$, and sheet resistance of 400 Ω/ . Unlike conventional AlGaN/GaN HEMTs, the dual-gate HEMT features a top gate electrode covering the main gate, separated by a 165-nm Si N dielectric layer. The top gate extends LFP =2 m toward the source and LFP =4 m toward the drain, as illustrated in Figure 1 Figure 1: see original paper. The dual-gate device includes a separate bonding pad for the top gate electrode, enabling independent signal control, as shown in Figure 1(b). The device dimensions are: gate width 100 m, gate length Lg=2 m, gate-source spacing 5 m, and gate-drain spacing 12 m.

Device Performance

The DC characteristics of the dual-gate HEMT are presented in Figure 2 [Figure 2: see original paper], showing a threshold voltage of -3.5 V, peak transconductance of 7.5 mS, maximum saturation drain current of 36 mA at Vg=1 V, and an on-resistance of 110 Ω. Dynamic characterization is performed with a 200 V drain bias applied by a high-voltage source meter, a load resistance Rd of 20 kΩ, and synchronized dual-channel pulsed control of the dual-gate electrodes at 0.24 MHz frequency, 50% duty cycle, and 0.1 s rise/fall times. The gate electrode is biased at +1 V in the on-state and -5 V in the off-state.

The on-state operation mode of the dual-gate device is defined as follows: the top gate is biased at 0 V in the off-state and at a positive voltage in the on-state. The input and output characteristic curves under this mode are shown in Figure 3 [Figure 3: see original paper]. The turn-on delay time is defined as the time required for the output voltage to reach 90% of its peak-to-peak value during the off-to-on transition. The on-state resistance is determined from the average voltage between 11 s and 12 s. When the dual-gate HEMT operates with the top gate as a source field plate (i.e., 0 V top-gate bias in on-state mode), the turn-on delay time is 1.6 s and the on-state resistance is 500 Ω. As the top-gate bias increases from 0 V to +30 V in on-state mode, the delay time and dynamic on-resistance decrease from 1.6 s and 500 Ω to 0.72 s and 415 Ω, respectively, as summarized in Table 1 .

Analysis and Modeling

During dynamic HEMT operation, defect states in the drift region capture negative charges under the strong electric field present in the off-state. In the on-state, these captured charges cannot be released quickly enough, forming a negative charge accumulation region that depletes electrons in the channel and causes the current collapse effect. Consequently, current collapse primarily occurs in the drift region. In the dual-gate HEMT, the top gate biased at 0 V during the off-state reduces electric field concentration and suppresses negative charge capture by defect states. During the on-state, the positive voltage applied to the top gate induces additional 2DEG, partially compensating for the 2DEG reduction caused by the negative charge region and thereby mitigating current collapse. The resistance model of the dual-gate device is illustrated in Figure 4 [Figure 4: see original paper].

$$R_{on_D} = 2R_{contact} + R_s + R_{channel} + \Delta R_{d1}//R_{d1} + R_{d2} \qquad (1)$$

The material sheet resistance is 400 Ω/ , the static drift region resistance R_d (R_ ×L_{gd}/W) is 48 Ω, and the total static resistance is 115 Ω, yielding 2R_{contact}+ R_s+ R_{channel} = 67 Ω. The top gate capacitance C_{TG} is 4.5×10 pF/cm², and the material electron mobility is 1080 cm²/V · s. V is the series resistance voltage division, calculated as 0.45 V.

Substituting these parameters into equations (1) and (2) yields the relationship between R_{d1}, R_{d2} and R_{ON_D}. Through fitting, R_{d1} and R_{d2} are determined, as shown in Figure 5 [Figure 5: see original paper]. R_{d1} is 80 Ω and R_{d2} is 330 Ω, corresponding to sheet resistances of 2000 Ω/ and 4125 Ω/ , respectively. This demonstrates that current collapse is more severe on the drain side of the drift region than on the gate side. Figure 6 [Figure 6: see original paper] shows the output current-voltage relationship during dynamic turn-on of the dual-gate device, with data taken from time t to t . When the top gate is biased at +30 V, the drain current is substantially higher than with 0 V top-gate bias. The turn-on drain current determines the device turn-on speed. Since the 2DEG induced by the positive top-gate voltage primarily compensates the on-resistance on the gate side of the drift region, the on-resistance value on the gate side of the drift region has a greater influence on the device’ s turn-on time.

Conclusion

The dual-gate AlGaN/GaN HEMT operating in on-state mode with positive top-gate bias demonstrates superior current collapse suppression compared to conventional source field-plate devices, achieving 55% and 17% reductions in turn-on delay time and dynamic on-resistance, respectively. Based on this operation mode, we developed a resistance model for the dual-gate HEMT and analyzed the distribution of dynamic resistance between the gate and drain electrodes through fitting. The results reveal that the on-resistance on the drain

side of the drift region has a more significant impact on the overall device on-resistance, whereas the on-resistance on the gate side of the drift region more strongly affects the device turn-on time.

Acknowledgments

We acknowledge the support and assistance from the Nano-Fabrication Facility and Testing and Analysis Platform at Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences!

References

[1] Binari S C, Ikossi K, Roussos J A, et al. Trapping effects and microwave power performance in AlGaN/GaN HEMTs [J]. IEEE Trans Electron Devices, 2001, 48 (3) : 465-471.
[2] Lee J S, Kim J W, Lee J H, et al. Reduction of current collapse in AlGaN/GaN HFETs using AlN interfacial layer [J]. Electron Lett, 2003, 39 (9) :750-751.
[3] Wu Y F, Saxler A, Moore M, et al. 30W /mm GaN HEMTs by field plate optimization [J]. IEEE Electron Device Lett, 2004, 25(3):117-119.
[4] Rongming Chu, Andrea Corrion, Mary Chen, et al. 1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic ON-Resistance [J]. IEEE Electron Device Lett., 2008, 32(5): 824-826.
[5] Sen Huang, Qimeng Jiang, Shu Yang, Chunhua Zhou, and Kevin J. Chen, Effective Passivation of AlGaN/GaN HEMTs by ALD-Grown AlN Thin Film [J], IEEE Electron Device Lett., 2012, 33: 516-518.

Figure 1 (a) Cross-sectional view of dual-gate AlGaN/GaN HEMT (DG-HEMT)
Figure 1 (b) Microscope image of the dual-gate device
Figure 2 (a) Device transfer characteristics
Figure 2 (b) Device output characteristics
Table 1 Relationship between fd and Ron_D and top-gate voltage in on-state
VTG_on_state (V) fd (s) Ron_D(Ω)
Figure 4 Resistance model diagram of dual-gate device
Figure 3 Device dynamic input and output characteristics
Figure 5 Measured and simulated on-resistance
Figure 6 Output current of device in on-state (Vg=1V) under dynamic testing

Note: Figure translations are in progress. See original paper for figures.

Source: ChinaXiv —Machine translation. Verify with original.