Experimental Study of Enhancement-Mode AlGaN/GaN HEMTs Realized by Ar Ion Implantation

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Abstract

GaN-based power transistors, represented by AlGaN/GaN HEMTs, have become a research focus in the field of power devices due to their advantages of wide bandgap, high operating junction temperature, high breakdown field strength, and high electron mobility. When GaN-based power transistors are applied in high-power switching circuits, normally-off characteristics are generally required for switching devices, i.e., enhancement-mode devices, for considerations of circuit design simplicity and safety. Ar ion implantation offers advantages of simple process, good repeatability, and stable controllability. This experiment investigates whether Ar ion implantation can realize enhancement-mode HEMT devices by adjusting the Ar ion implantation energy and dose, while simultaneously studying the effect of LP-SiNx as an energy blocking layer. Experimental results demonstrate that Ar ion implantation can achieve enhancement-mode operation, but suffers from low saturation current. Annealing can repair implantation damage and improve saturation current to a certain extent. Employing LP-SiNx as an energy blocking layer can reduce damage and relatively increase saturation current, but exhibits a hysteresis problem. As a method for realizing enhancement-mode devices, Ar ion implantation still requires further investigation and improvement.

Full Text

Preamble

Experimental Study on Enhancement-Mode AlGaN/GaN HEMT Devices Based on Ar Ion Implantation

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Abstract

GaN-based power transistors, exemplified by AlGaN/GaN HEMTs, have become a focal point in power device research due to their wide bandgap, high operating junction temperature, high breakdown field strength, and high electron mobility. When GaN-based power transistors are applied to high-power switching circuits, enhancement-mode operation (normally-off behavior) is generally required for simplified circuit design and safety considerations. Ar ion implantation offers advantages of simple process, good repeatability, and stable controllability. This study investigates whether enhancement-mode HEMT devices can be achieved through Ar ion implantation by adjusting the implantation energy and dose, while also examining the effectiveness of LP-SiNx as an energy blocking layer. Experiments demonstrate that Ar ion implantation can realize enhancement-mode operation, but suffers from small saturation current issues. Annealing can repair implantation damage and improve saturation current to some extent. Using LP-SiNx as an energy blocking layer reduces lattice damage and relatively increases saturation current, but introduces hysteresis problems. As a method for achieving enhancement-mode operation, Ar ion implantation requires further research and improvement.

Keywords

AlGaN/GaN HEMT, Ar ion implantation, enhancement-mode

With technological advancement, HEMT devices have found increasingly widespread applications. When HEMT devices employ III-nitride semiconductors, high-concentration two-dimensional electron gas (2DEG) can form at heterostructures such as AlGaN/GaN due to piezoelectric and spontaneous polarization effects. Additionally, III-nitride semiconductor HEMTs offer high insulating breakdown field strength and excellent high-temperature characteristics. HEMTs with III-nitride heterostructures can serve not only as high-frequency devices but also as power switching devices for high-voltage, high-current applications. In high-power switching circuits, enhancement-mode operation (normally-off characteristic) is generally required for simplified circuit design and safety considerations.

Currently, common methods for realizing enhancement-mode HEMT devices include thin barrier layers, p-type gate structures, recessed gate structures, fluorine plasma treatment, and fluorine ion implantation. Each of these techniques has certain drawbacks. The world' s first enhancement-mode HEMT was implemented using a thin barrier layer. This method avoids etching processes and thus introduces minimal damage, but results in small saturation current due to the thin barrier. To address this issue, recessed gate structures were developed based on thin-barrier enhancement-mode HEMTs. While recessed gate struc-

tures solve the small saturation current problem, the barrier layer in typical HEMTs is only 20-30 nm, making the etching process difficult to control and resulting in poor repeatability. P-type cap layers avoid etching but generate interface states that affect device stability. Fluorine plasma treatment can also achieve enhancement-mode HEMTs without etching, but the presence of plasma during fluorine ion injection causes etching of the barrier layer. Additionally, since multiple ion species exist in the plasma, control is difficult in experiments. Furthermore, because fluorine ions are charged, reliability issues inevitably arise.

The purpose of using Ar ion implantation is to disrupt the AlGaN crystal lattice, weakening polarization and thereby depleting the 2DEG under the gate to achieve enhancement-mode operation. Compared with other enhancement-mode implementation methods, Ar ion implantation offers advantages of simple process, good repeatability, and stable controllability.

1. Device Fabrication and Process

(1) The substrate surface is treated in the reaction chamber.

(2) AlGaN/GaN epitaxial layers are grown on the substrate, with GaN thickness of 1 m-3 m and AlGaN thickness of 14 nm-30 nm, where the Al mole fraction is 20%-30%.

(3) Mesa isolation is performed using ion implantation.

(4) Ohmic contacts for source and drain electrodes are formed through photolithography and metal deposition of Ti/Al/Ni/Au with thicknesses of 20 nm/130 nm/50 nm/150 nm, respectively, followed by lift-off and annealing at 890°C for 30 seconds.

(5) Ar ion implantation is performed using an ion implanter.

(6) Ni/Au gate metal layers are deposited through photolithography and metal evaporation with thicknesses of 50 nm/250 nm, respectively.

(7) Annealing at 400°C for 30 minutes is performed to repair damage caused by Ar ion implantation.

The fabricated devices have a gate length of 4 m, gate-source spacing of 4 m, gate-drain spacing of 7 m, gate width of 100 m, and Ar ion implantation region length of 2 m.

2. Experimental Results and Discussion

Transfer characteristics were measured using an Agilent B1505A semiconductor parameter analyzer with a drain-source voltage of 10 V. Prior to implantation, simulations were performed to select appropriate implantation energies.

The first Ar ion implantation experiment was conducted without an energy blocking layer at an implantation energy of 10 keV with doses of 10^14 cm^-2, 10^13 cm^-2, and 10^12 cm^-2.

The transfer curve for a dose of 10^14 cm^-2 is shown in Figure 1 Figure 1: see original paper, and after 400°C annealing in Figure 1(b). Enhancement-mode operation is achieved, but the current is extremely small, remaining in the microampere range even after annealing, suggesting excessive damage from Ar ion implantation.

The transfer curve for a dose of 10^13 cm^-2 is shown in Figure 2 Figure 2: see original paper, and after 400°C annealing in Figure 2(b). Enhancement-mode operation is achieved, and annealing significantly improves the saturation current to the milliampere range. However, this is still substantially lower than that of depletion-mode devices, reaching only one-seventh to one-eighth of the depletion-mode saturation current.

The transfer curve for a dose of 10^12 cm^-2 is shown in Figure 3 [Figure 3: see original paper]. Although reducing the implantation dose increases the saturation current, enhancement-mode operation is not achieved; the threshold voltage is merely shifted to the right.

The second Ar ion implantation experiment employed a 20 nm LP-SiNx energy blocking layer with an implantation energy of 20 keV and doses of 10^14 cm^-2 and 10^15 cm^-2.

The transfer curve for a dose of 10^14 cm^-2 is shown in Figure 4 Figure 4: see original paper, and after 400°C annealing in Figure 4(b). This method achieves enhancement-mode operation with relatively large saturation current, but exhibits significant step-like hysteresis.

The transfer curve for a dose of 10^15 cm^-2 is shown in Figure 5 Figure 5: see original paper, with no obvious change after 400°C annealing. After 500°C annealing, as shown in Figure 5(b), enhancement-mode operation is achieved, but the higher dose causes severe lattice damage.

Experiments demonstrate that Ar ion implantation is a feasible method for achieving enhancement-mode operation, with threshold voltage tunable through adjustment of implantation energy and dose. Using LP-SiNx as an energy blocking layer effectively reduces ion implantation damage to the lattice and increases saturation current, though the resulting hysteresis requires resolution. Furthermore, issues such as saturation current reduction and reliability degradation caused by Ar ion implantation necessitate further investigation.

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Note: Figure translations are in progress. See original paper for figures.